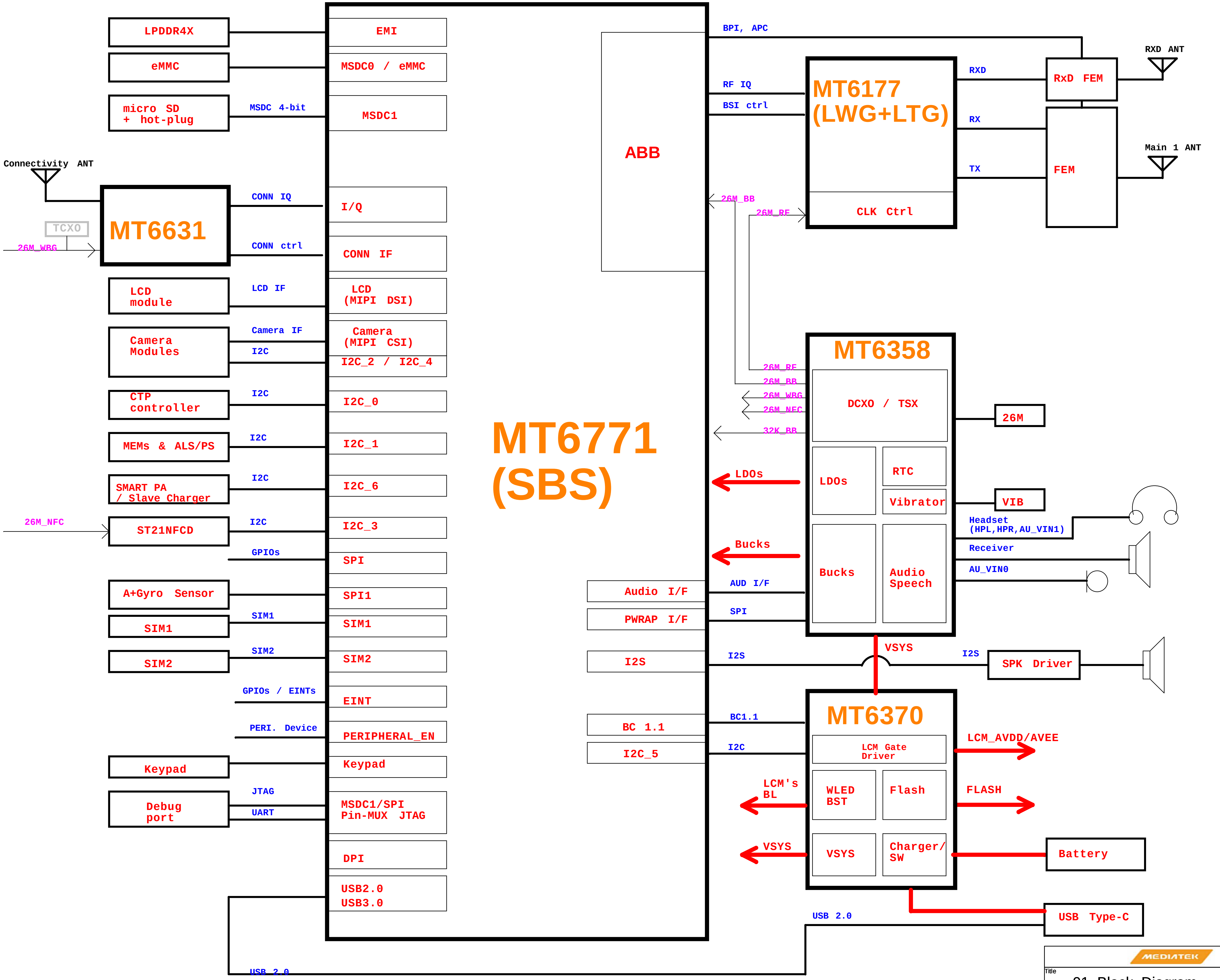
Project : MT6771 LPDDR4X REF_SCH TOP LEVEL



MEDIATEK

Title: 01_Block_Diagram

Size: C — MTK Confidential

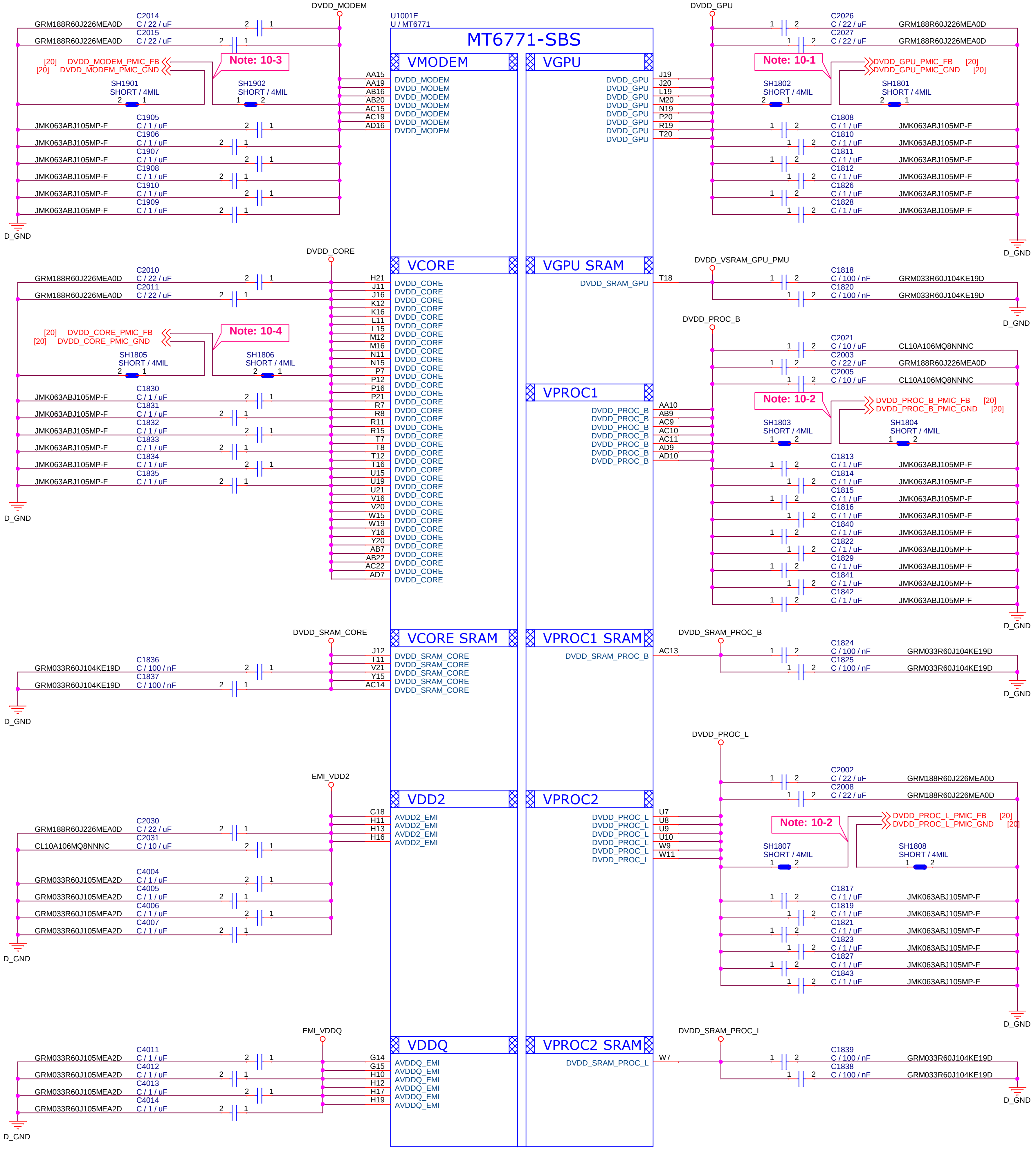
Date: Thursday, January 25, 2018 — Sheet 01 of 99

I2C	AP, SCP, SSPM	Function	I2C Spec.	Budget Timing	I2C Slave Address (7-bit mode)
I2C-0	AP	CTP	400 Kbps	Yes.	GT1151 I2C address: 0X5D (Write:0xBA, Read:0xBB) or 0x14 (Write:0x28, Read:0x29)
I2C-1(I3C)	AP ,SCP	M Sensor	400 Kbps	Yes.	AK09915C / M-Sensor I2C Address 0x0C (Write: 0x18, Read: 0x19)
		RGB / PS Sensor	400 Kbps	Yes.	CM36558 / UV + PS I2C address: 0X51 (Write:0xA2, Read:0xA3) - default CM36652 / RGB + PS I2C address: 0X60 (Write:0xC0, Read:0xC1
		Barometer	400 Kbps	Yes.	BMP280 I2C address: 0X77 (Write:0xEE, Read:0xEF)
I2C-2 (I3C)	AP	Rear Camera - 21M	400 Kbps		Rear camera I2C address: 0X1A (Write:0x34, Read:0x35) AF driver I2C address: 0X0C (Write:0x18, Read:0x19) EEPROM I2C address: 0X50 (Write:0xA0, Read:0xA1)
		Dual camera module Rear Camera - 16M	400 Kbps	Yes.	Rear camera I2C address: 0X (Write:0x, Read:0x) AF driver I2C address: 0X (Write:0x, Read:0x) EEPROM I2C address: 0X (Write:0x, Read:0x)
I2C-3	AP	NFC	400K bps	Yes.	NFC I2C address: 0X08 (Write:0x10, Read:0x11)
I2C-4 (I3C)	AP	Front Camera - 5M	400 Kbps	Yes.	Front camera I2C address:0X35 (Write:0x6A, Read:0x6B) EEPROM I2C address: 0X54 (Write:0xA8, Read:0xA9)
		Dual camera module Rear Camera - 20M	400 Kbps	Yes.	Rear camera I2C address: 0X (Write:0x, Read:0x) AF driver I2C address: 0X (Write:0x, Read:0x) EEPROM I2C address: 0X (Write:0x, Read:0x)
I2C-5	SSPM	MT6370	3.4Mbps	Yes.	MT6370 PD's I2C address: 0X4E (Write:0X9C, Read:0X9D) MT6370 PMU's I2C address: 0X34 (Write:0X68, Read:0X69)
I2C-6	AP ,SCP	Smart PA	400 Kbps	Yes.	RT5509 Speaker AMP I2C Address: 0x34 (Write:0x68, Read:0x69)
		Slave charger	400 Kbps	Yes.	RT9465 / slave charger I2C address: 0X4B (Write:0x96, Read:0x97)

Note : I2C Spec. : Standard mode (100 kbps) and Fast mode (400 kbps), Fast mode Plus (1 Mbps) and High-speed mode (3.4 Mbps)

Date	Category	Item
2017.09.15 (V0.1)	Page 05	V0.1 Release
2017.09.29 (V0.2)	Page 20	1. Reduce voltage rating of C2017 to 10V rating 2. Remove C2150 because of latest MT6358 constraint
	Page 21	1. C2111 (VXO22_PMU) is reduced from 2.2uF to 1uF 2. Remove C2150 because of latest MT6358 constraint
	Page 26	1. Reduce voltage rating of C2605 to 6.3V rating Reduce voltage rating of C2603 to 10V rating Reduce voltage rating of C2601 to 25V rating 2. Update ESD2602 to AZ4507
	Page 27	Reduce voltage rating of C2704, C2706 to 6.3V rating
	Page 29	Reduce voltage rating of C2904 to 6.3V rating Reduce voltage rating of C2901 to 25V rating
	Page 31	1. Remove R3104, and set G1 pin of U3101 NC 2. Reduce voltage rating of C3113, C3114 to 6.3V rating
	Page 32	1. Update U3201 P/N 2. Change R3207 to short pad SH3207 with 10 mil width suggestion Change R3212 to short pad SH3212 with 60 mil width suggestion 3. Reduce voltage rating of C3267, C3270 to 6.3V rating Reduce voltage rating of C3205, C3228, C3230, C3234, C3239 to 10V rating Reduce voltage rating of C3222, C3225, C3233, C3238 to 16V rating 4. Reduce component size of C3229 from 0603 to 0402 size
	Page 33	Reduce voltage rating of C3307 to 16V rating
	Page 50	Reduce voltage rating of C5005, C5009, C5018 to 16V rating
	Page 62	Reduce voltage rating of C6220 to 16V rating Reduce voltage rating of C6225 to 16V rating
	Page 63	Reduce voltage rating of C6313 to 16V rating
	Page 65	Reduce voltage rating of C6503 to 6.3V rating
	Page 69	Reduce voltage rating of C6910 to 6.3V rating
	Page 71	1. Update ESD7102 to AZ4514-01F 2. For ESD7103 and ESD7104, please refer to related design guide
2017.11.16 (V0.3)	Page 11	1. Change power of AVDD18_DDR(G9) and AVDD18_PLLGP(AB13) from VIO18_PMU to EMI_VDD1 2. Connect below analog power pad of SOC to AVDD18_SOC in star connection to SH2101 AVDD18_MD (AH19), AVDD18_AP (AH21), AVDD18_USB (F27), AVDD18_SSUSB (H23) AVDD18_WBG (B2), AVDD18_UFS (D23), AVDD18_CPU (AC7)
	Page 12	1. Add BPI_BUS3, BPI_BUS4, BPI_BUS5, BPI_BUS6 for RF eLNA application 2. Add Note 12-5 for DRAM type bootstrap and update Note 12-1 for IOJTAG function
	Page 21	1. C2111 (VXO22_PMU) is updated from 1uF to 2.2uF 2. Add SH2101 for star connection between AVDD18_SOC and VIO18_PMU 3. Add note for VS2_LDO4
	Page 28	Add External 1.8V LDO, U2800, for LPDDR4X 1.8V and add C2820, C2821 for external 1.8V LDO (U2800) related schematic
	Page 35	Add page 35 for RF eLNA application, and please refer to MT6177 design notice for further detail
	Page 44	Change power of eMCP VDD1 from VIO18_PMU to EMI_VDD1
	Page 77	Add Note 77-7 for customer design on sensor application

Date	Category	Item
2017.11.16 (V0.3)	Page 62	1. Change Audio to ACC mode 2. Change R6229 to C6229 with C / 1 / uF, R6230 to C6230 with C / 1 / uF, R6231 to C6233 with C / 4.7 / uF 3. Change R6225 to R / 0 / ohm, R6209 to R / 1 / K, R6210 to R / 1.5 / K, R6219 to R / 2.49 / K / NC
	Page 63	1. Change Audio to ACC mode 2. Change R6326 to C6326 with C / 1 / uF, R6325 to C6325 with C / 1 / uF, R6323 to C6323 with C / 1 / uF 3. Change R6324 to C6322 with C / 1 / uF
2017.11.21 (V0.4)	Page 11	Change power of AVDD18_PLLGP(AB13) from EMI_VDD1 to AVDD18_SOC in star connection to SH2101
2017.12.29 (V1.0)	Page 11	Remove reserved cap., C7103, for AVDD18_USB, and, C7209, for AVDD18_SSUSB
	Page 20	1. Change C2017 from 1uF 0603 to 2.2uF 0402 for noise reduction 2. Remove reserved components C2006 and VR2001
	Page 21	1. Remove reserved component C2128 2. Add Note 21-2 for notice of LDO layout constraint
	Page 22	Remove reserved components C2201 and R2201
	Page 32	Modify VPA mid cap size, C3230, from 0603 to 0402
	Page 44	1. Update eMCP, U4401, from H9HP52ACPMMDAR-KMM to KMDH6001DM-B422 2. Add C4427 with 100 nF and C4428 with 2.2uF for VDD1 of LPDDR4X, please also check with DRAM vendor sugestion 3. Remove short pad SH4405
	Page 51	To enrich AGC saturation margin, add 3dB resistor attenuator at external LNA output 1. Change R5011 from 0 ohm to 18 ohm 2. Change C5029 from NC to 300 ohm 3. Change C5030 from NC to 300 ohm
	Page 77	1. Add R7701 to reserve RC filter for VDD noise suppression of A+G sensor 2. Update C6401 from C / 100 / nF to C / 1 / uF
2018.1.10 (V1.1)	Page 77	Change A+G Solution, U6404, from LSM6DS3TR-C to BMI160
2018.1.14 (V1.2)	Page 13	Connect CSI ports which are no use to GND
2018.1.23 (V1.21)	Page 13	Add Note 13-1



Schematic design notice of "10_BB_POWER_PDN" page.

Note 10-1: Differential pair of DVDD_GPU remote sense must be close to BB's ball.

Remote sense trace with GND shielding to PMIC (Differential)

Note 10-2: Differential pair of DVDD_PROC remote sense must be close to BB's ball

Remote sense trace with GND shielding to PMIC (Differential)

Note 10-3: Differential pair of DVDD_MODEM remote sense must be close to BB's ball.

Remote sense trace with GND shielding to PMIC (Differential)

Note 10-4: Differential pair of DVDD_CORE remote sense must be close to BB's ball.

Remote sense trace with GND shielding to PMIC (Differential)

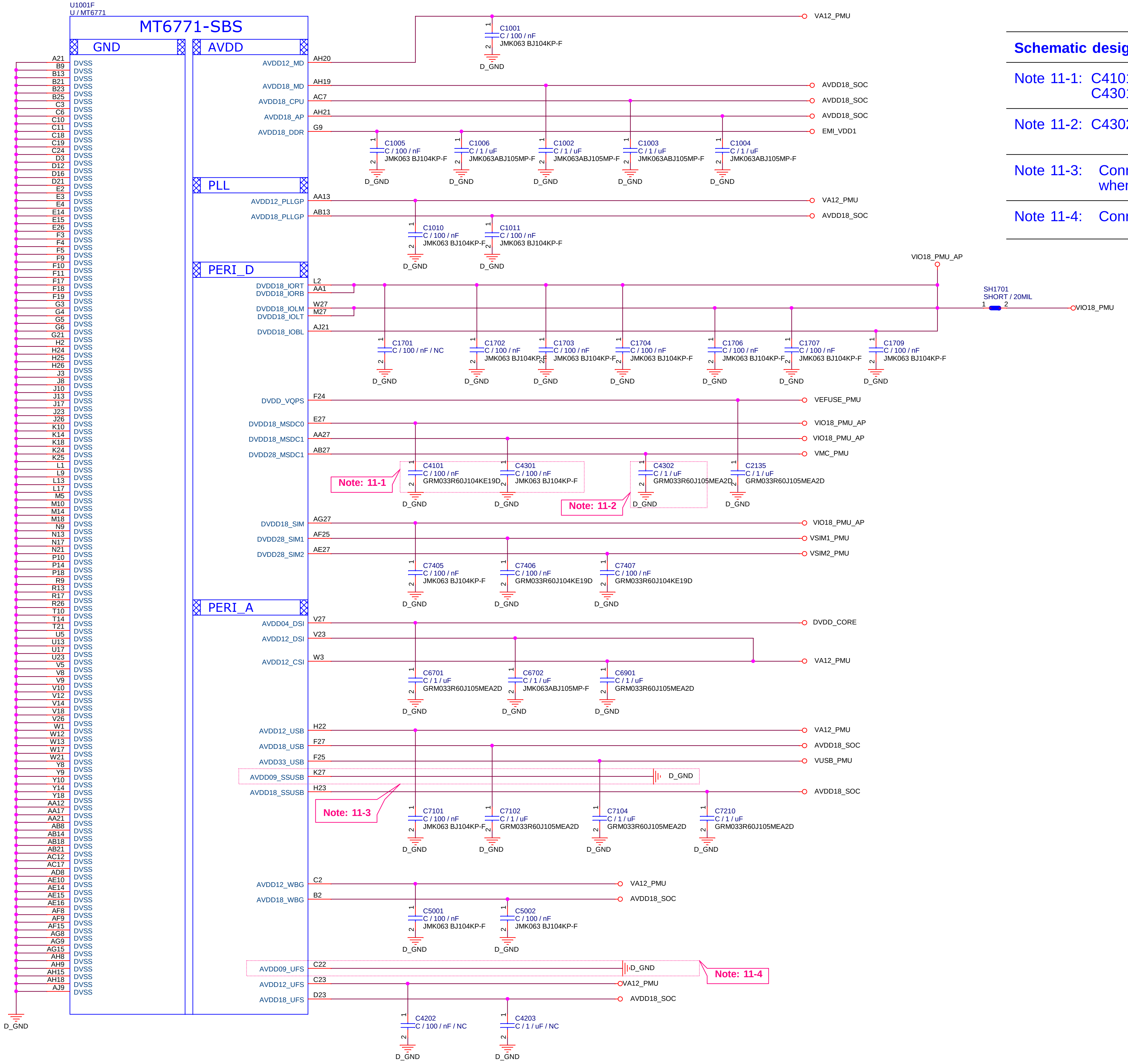
MEDIATEK

Title: 10_BB_POWER_PDN

Size: C

MTK Confidential

Date: Thursday, January 25, 2018 Sheet 10 of 99



Schematic design notice of "11_BB_POWER_IO" page.

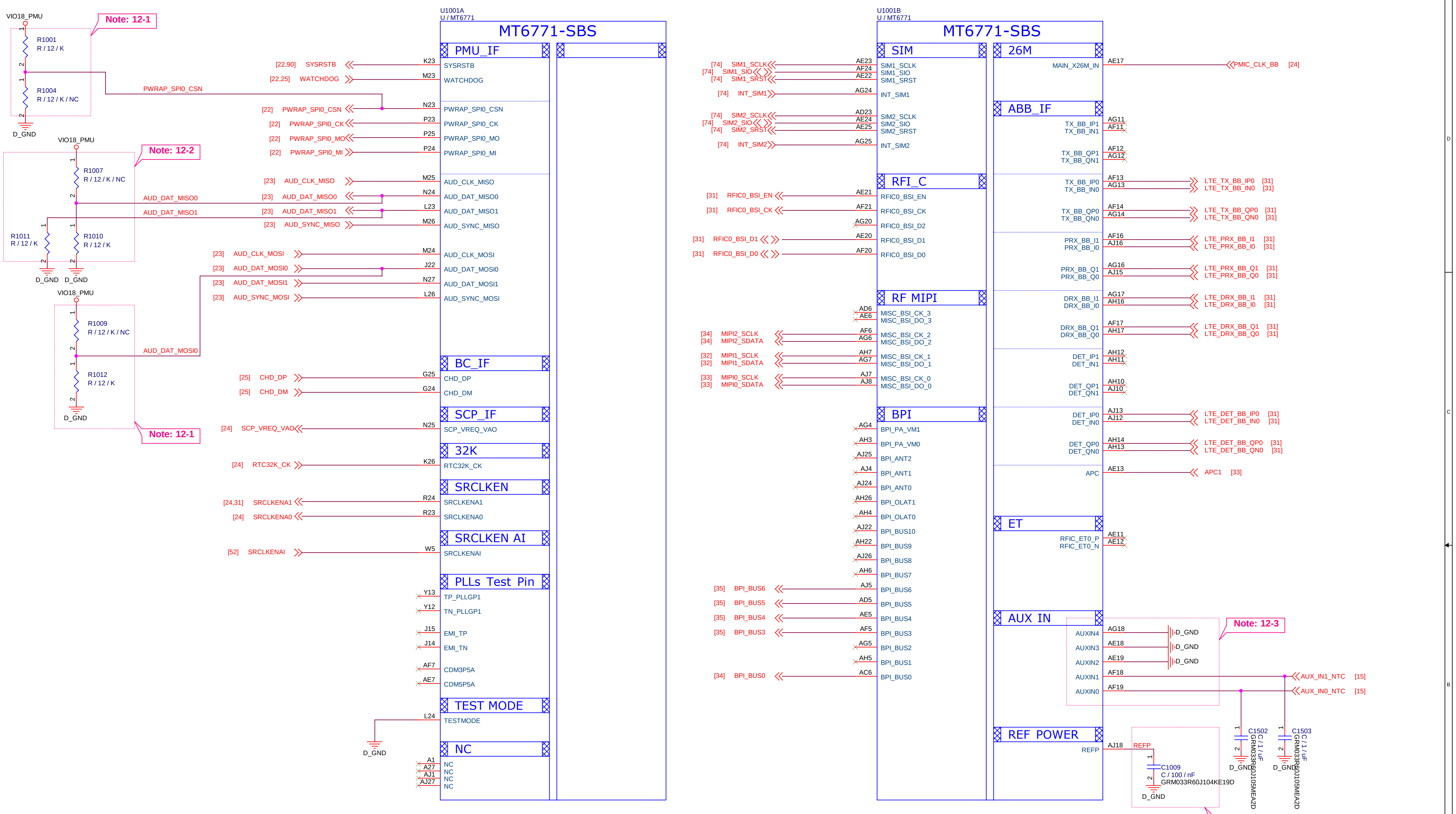
Note 11-1: C4101 closed DVDD18_MSDC0 150mil
C4301 closed DVDD18_MSDC1 150mil

Note 11-2: C4302 closed DVDD28_MSDC1 150mil

Note 11-3: Connects "AVDD09_SSUSB" to GND when USB3.0 is not used.

Note 11-4: Connects "AVDD09_UFS" to GND when UFS is not used.

Title	11_BB_POWER_PDN
Size C	MTK Confidential
Date: Thursday, January 25, 2018	Sheet 11 of 99



Schematic design notice of "12_BB_1" page.

Note 12-1: "PWRAP_SPI0_CSN" and "AUD_DAT_MOSI0" are bootstrap pins to select which interface will be the JTAG pin out.

PWRAP_SPI0_CSN	AUD_DAT_MOSI0	AP_JTAG	IO_JTAG
HI	LO	N/A	N/A
HI	HI	SPI_CSB/SPI_CLK/ SPI_MO/SPI_MI/EINT8	N/A
LO	LO	SPI_CSB/SPI_CLK/ SPI_MO/SPI_MI/EINT8	DPI_11/DPI_HSYNC/DPI_VSYNC/DPI_DE/ DPI_CK/DPI_D8/DPI_D9
LO	HI	MSDC1_CLK/CMD/ DAT0/DAT1/DAT2	N/A

Note 12-2: "AUD_DAT_MISO0" is bootstrap pin to enable serial JTAG output over USB2.0 interface or not.
When "AUD_DAT_MISO0" is pulled to high in system start up and then USB2.0 interface will be switched into serial JTAG mode.

"AUD_DAT_MISO1" is bootstrap pin to select system booting up from eMMC or UFS device.

AUD_DAT_MISO1	Booting device
LO	eMMC
HI	UFS

Note 12-3: To shunt a 1uF capacitor in the AUXIN ADC input to prevent noise coupling. It should be placed as close to BB as possible. Connect the unused AUX ADC input to GND.

Note 12-4: The de-coupling cap. for REFP (AJ18 ball) have to be placed as close to BB as possible.

Note 12-5: AUD_SYNC_MISO and AUD_CLK_MISO are DDR type feature in bootstrap

AUD_SYNC_MISO	AUD_CLK_MISO	DDR
LO	LO	LPDDR4X
LO	HI	LPDDR4X(Ext x 2 EN)
HI	LO	LPDDR3
HI	HI	LPDDR4X(Ext x 1 EN)

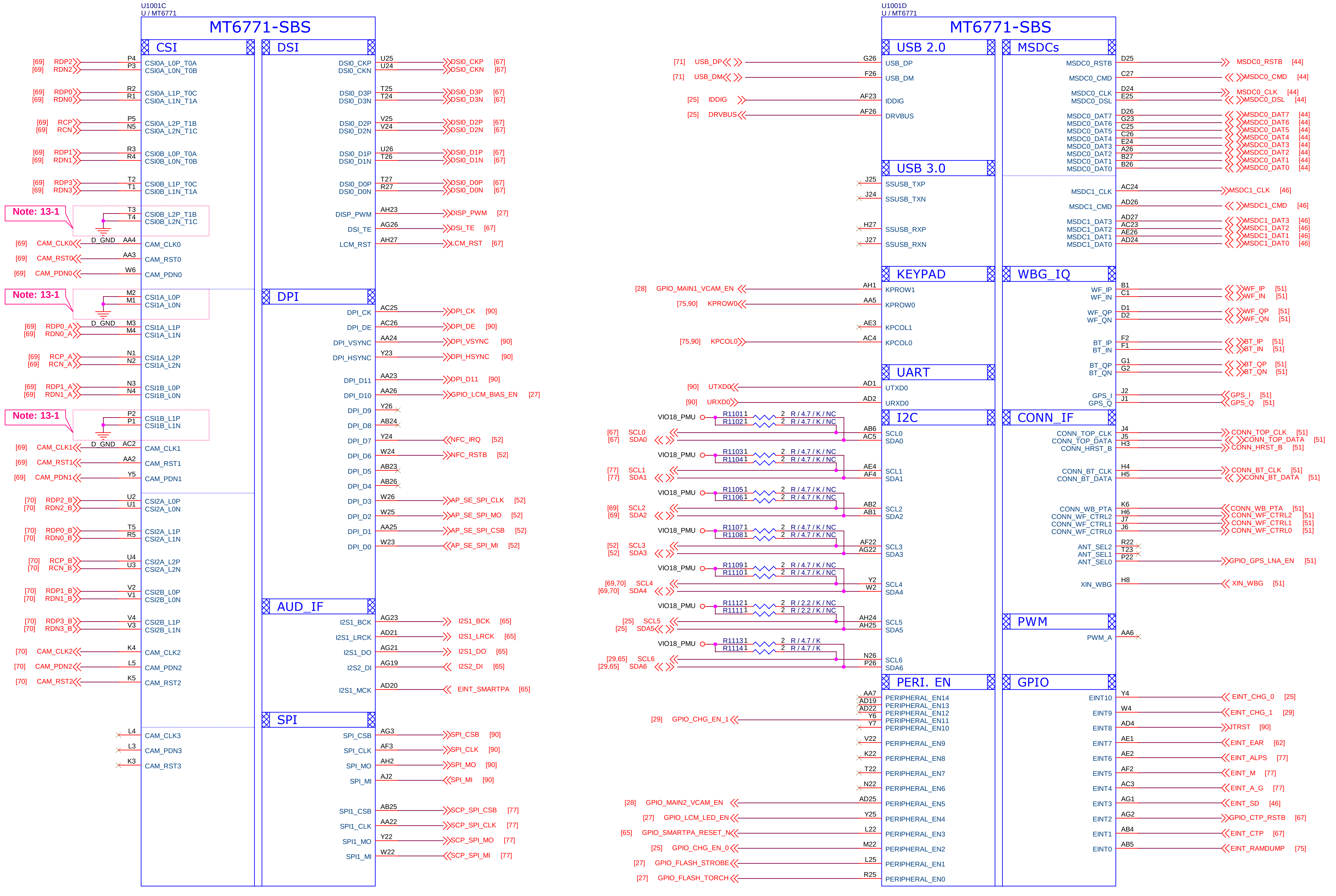
MEDIATEK

Title: 12_BB_1

Size: C

MTK Confidential

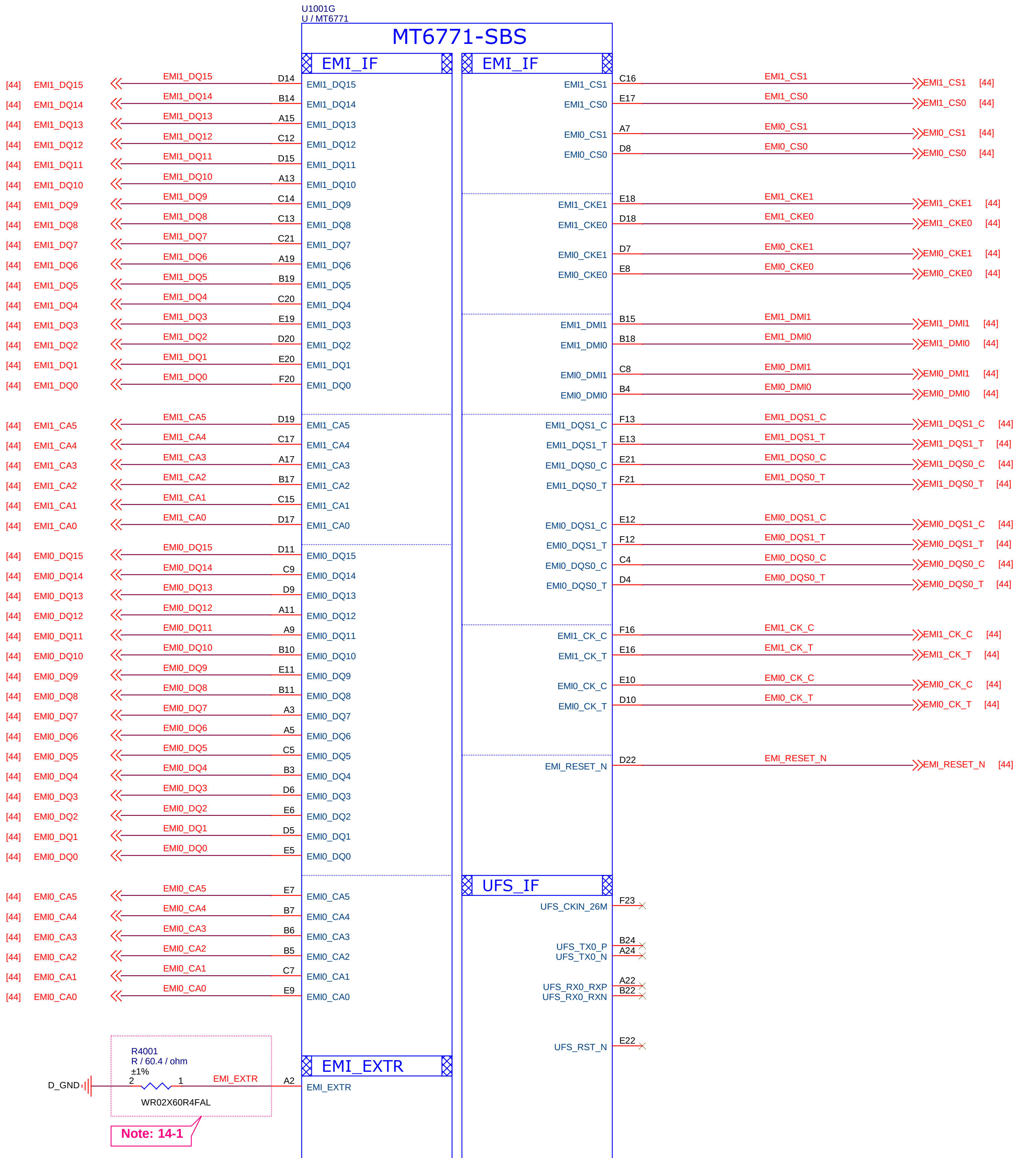
Date: Thursday, January 25, 2018 Sheet 12 of 99



Schematic design notice of "13_BB_2" page.

Note 13-1: CSI ports which are no use could be connected to GND or set in NC.
For detail information, please refer to MT6771 Design Notice

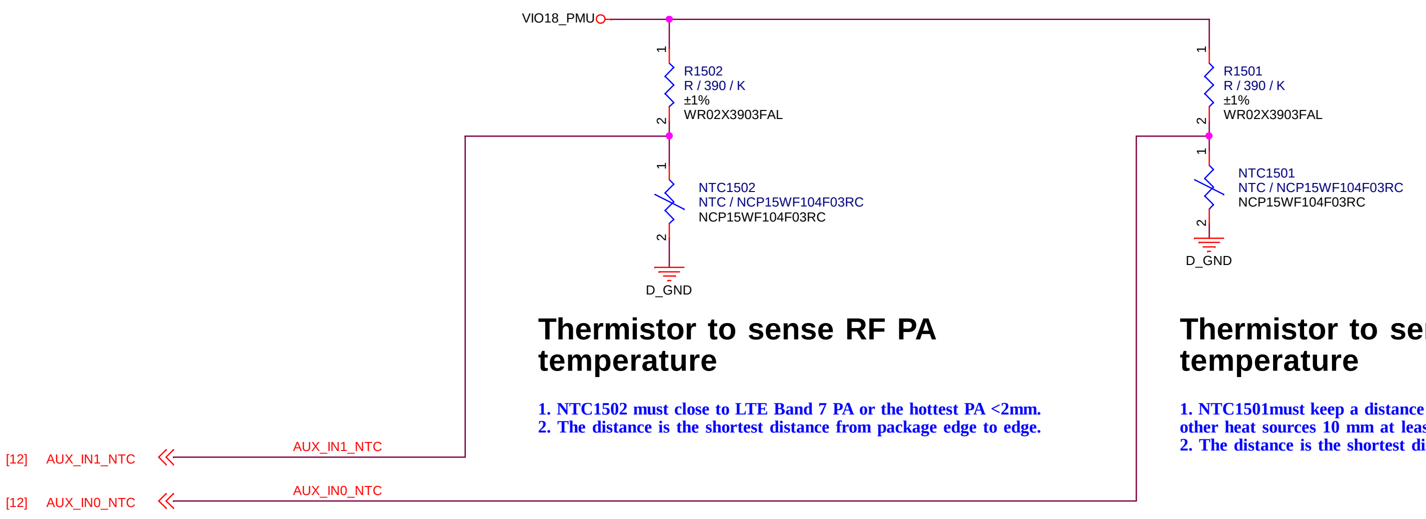
Title	13_BB_2
Size C	MTK Confidential
Date: Thursday, January 25, 2018	Sheet 13 of 99



Schematic design notice of "14_BB_3" page.

Note 14-1: The resistor of EMI_EXTR for DRAM has to be placed near to BB as close as possible
R4001, please select 60.4 ohm 1% resistor

Title	14_BB_3
Size C	MTK Confidential
Date: Thursday, January 25, 2018	Sheet 14 of 99



Thermistor to sense RF PA temperature

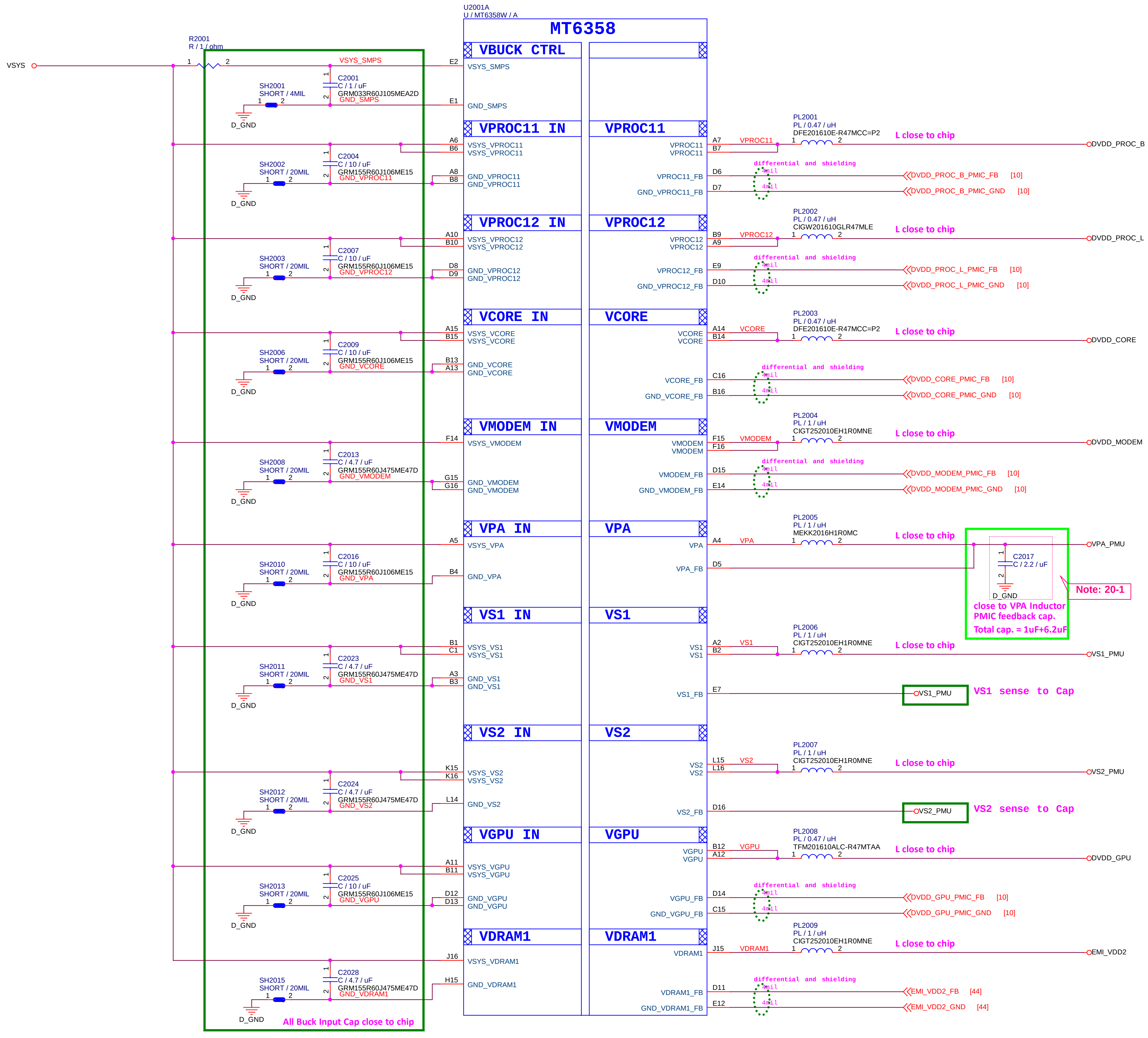
1. NTC1502 must close to LTE Band 7 PA or the hottest PA <2mm.
2. The distance is the shortest distance from package edge to edge.

Thermistor to sense AP temperature

1. NTC1501must keep a distance about 6~8 mm away from AP and far from other heat sources 10 mm at least.
2. The distance is the shortest distance from package edge to edge.

MEDIATEK

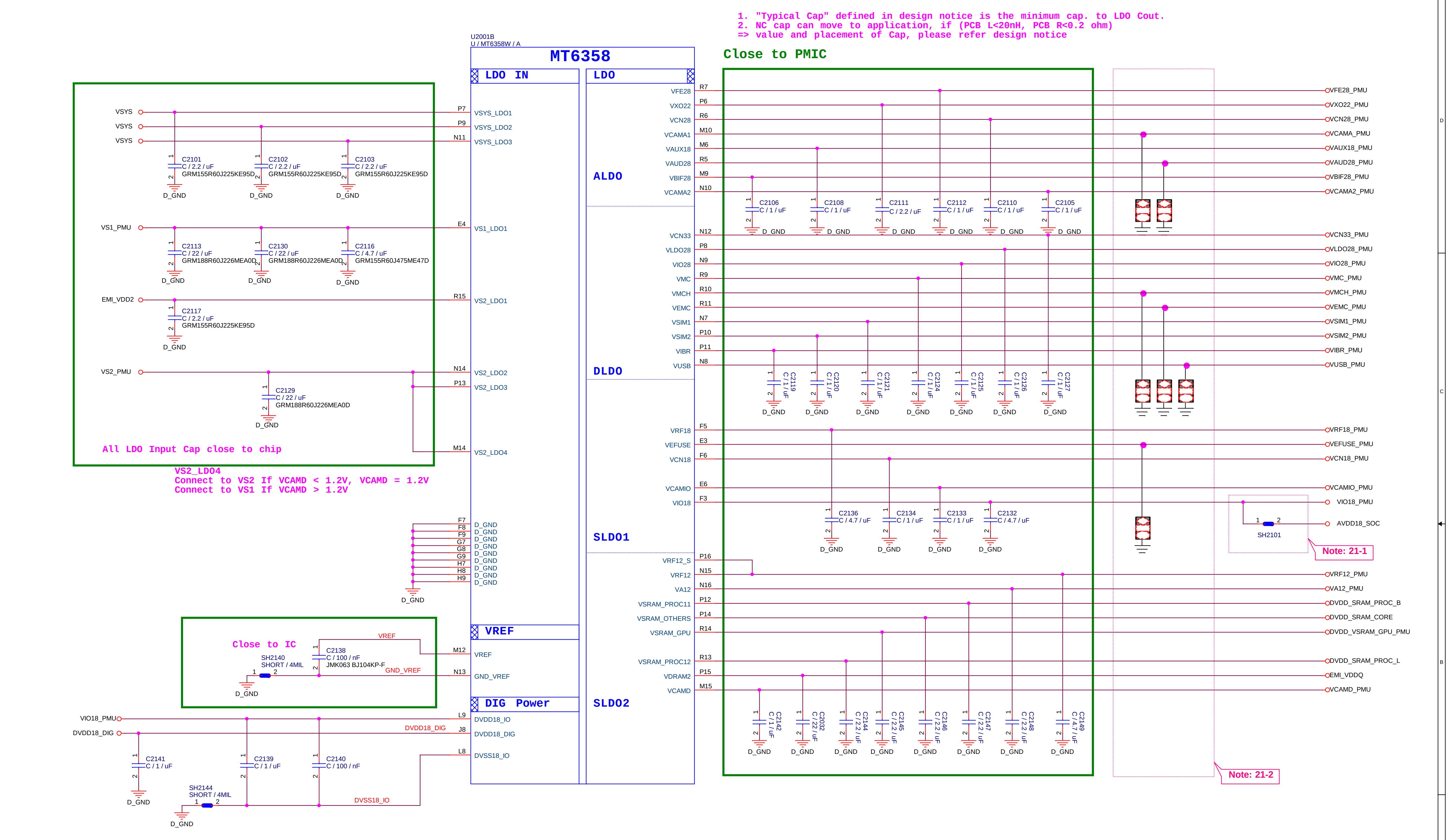
Title	15_BB_AUXADC_Thermal
Size C	MTK Confidential
Date: Thursday, January 25, 2018	Sheet 15 of 99



Schematic design notice of "20_POWER_MT6358-Buck" page.

Note 20-1: Please select C2017 with 0402 size

Title	20_POWER_MT6358-Buck
Size C	MTK Confidential
Date: Thursday, January 25, 2018	Sheet 20 of 99



Schematic design notice of "21_POWER_MT6358-LDO" page.

Note 21-1: Please set SH2101 close to C2132, making star connection between VIO18_PMU and AVDD18_SOC near to LDO cap. C2132
Please also refer to MT6358 design notice for further detail design information

Note 21-2: If these power trace can meet LDO layout constraint, these CAP can be NC or removed.
Please refer to MT6358 design notice.

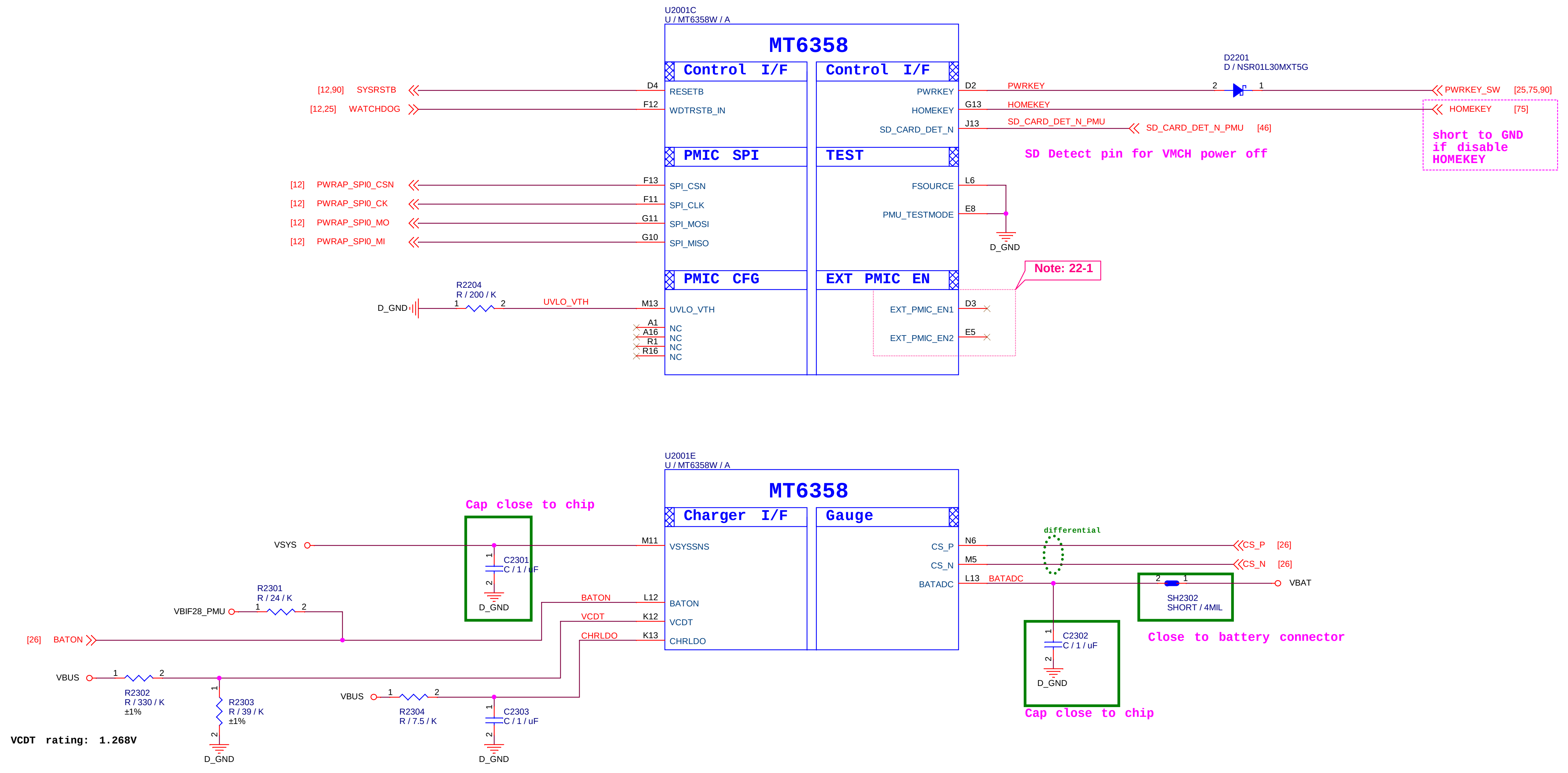
MEDIATEK

Title: 21_POWER_MT6358-LDO

Size: C

MTK Confidential

Date: Thursday, January 25, 2018



Schematic design notice of "22_POWER_MT6358-General"

Note 22-1: EXT_PMIC_EN1 : For UFS_1V8, and keep floating if it is not used
EXT_PMIC_EN2 : For VA09 of SSUSB/UFS, and keep floating if it is not used

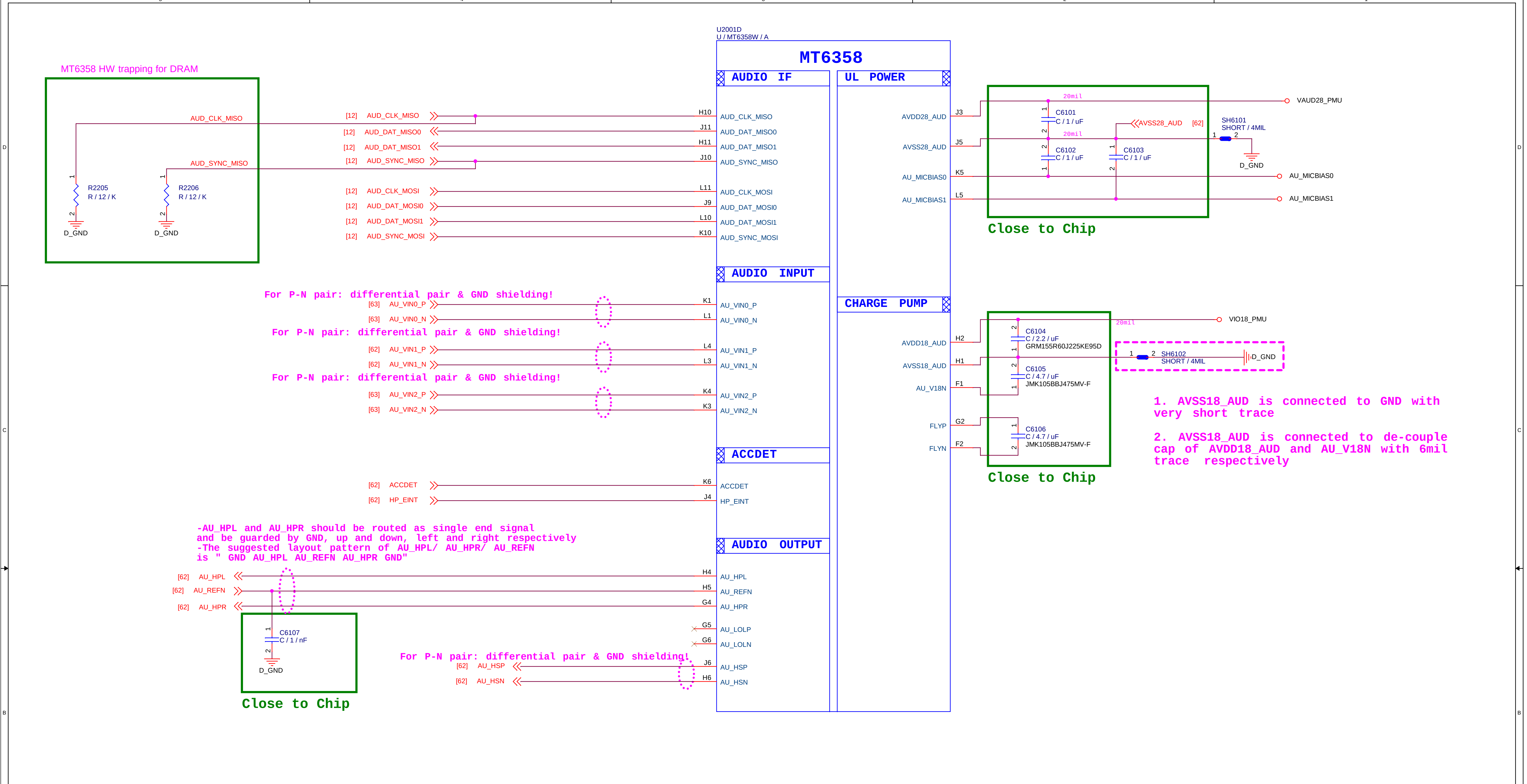
MEDIATEK

Title: 22_POWER_MT6358-IF

Size: C

MTK Confidential

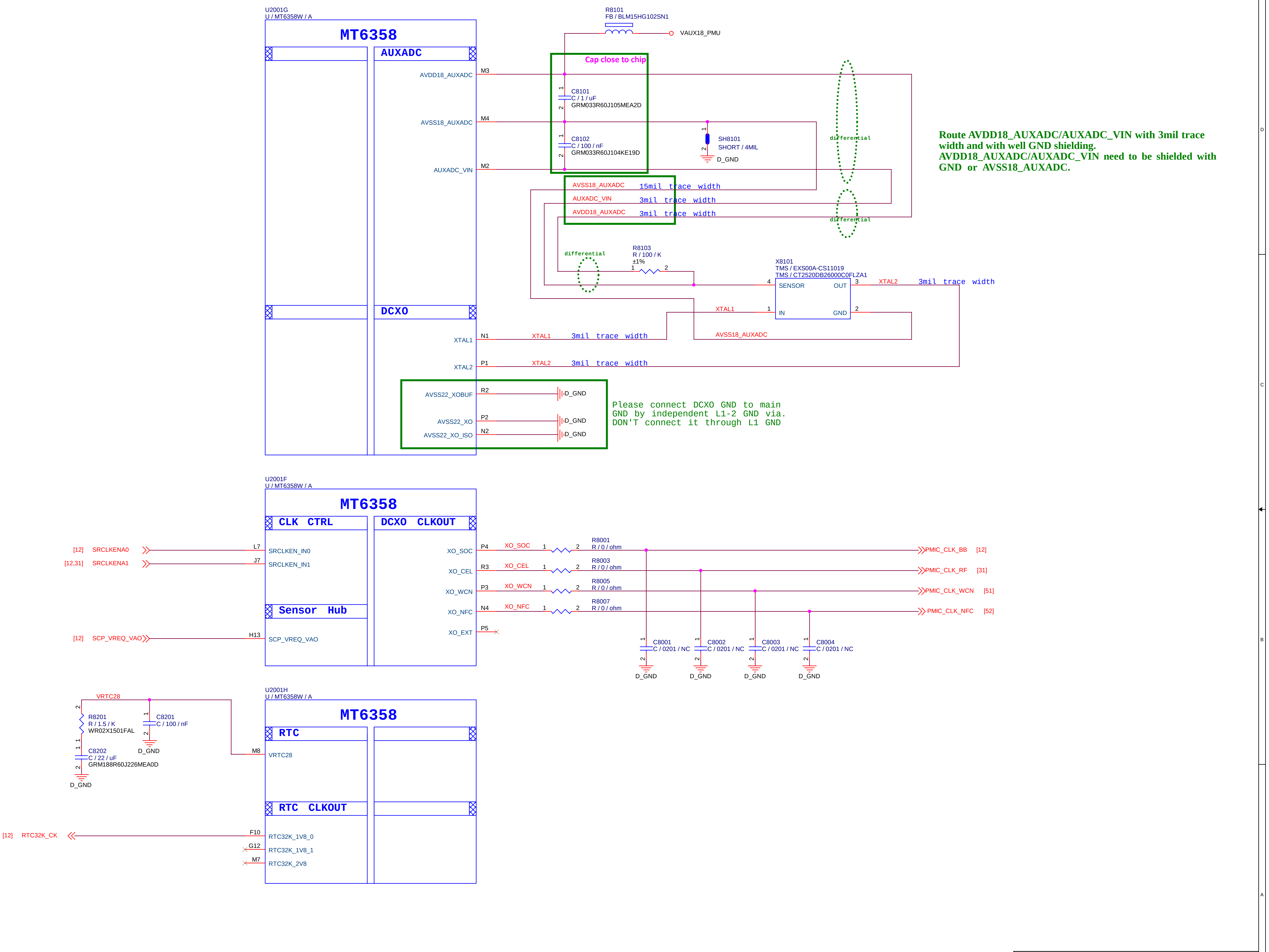
Date: Thursday, January 25, 2018 | Sheet 22 of 99



Schematic design notice of "23_POWER_MT6358-Audio"

Note 23-1: VDRAM 2 / VDRAM1 output voltage vs. trap pin.

HW GPIO configuration		Trapping Option		DRAM type	VDRAM2 Power source (VS2_LDO1_ball)
AUD_SYNC_MISO	AUD_CLK_MISO	VDRAM1	VDRAM2		
0	0	1.125V	0.6V	LP4X	VDRAM1
0	1	OFF	1.8V	LP4X (Ext x 2 EN)	VS1
1	0	1.225V	OFF	LP3	VDRAM1
1	1	1.125V	1.8V	LP4X (Ext x 1 EN)	VS1



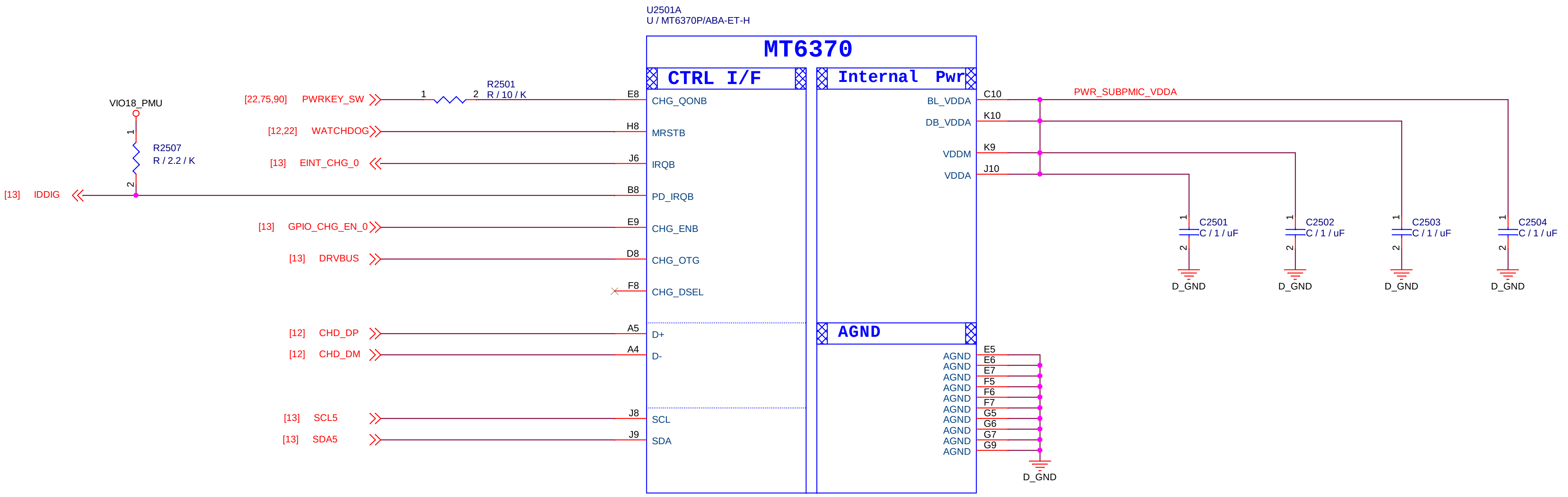
MEDIATEK

Title
24_POWER_MT6358_Clock

Size C

MTK Confidential

Date: Thursday, January 25, 2018 Sheet 24 of 99

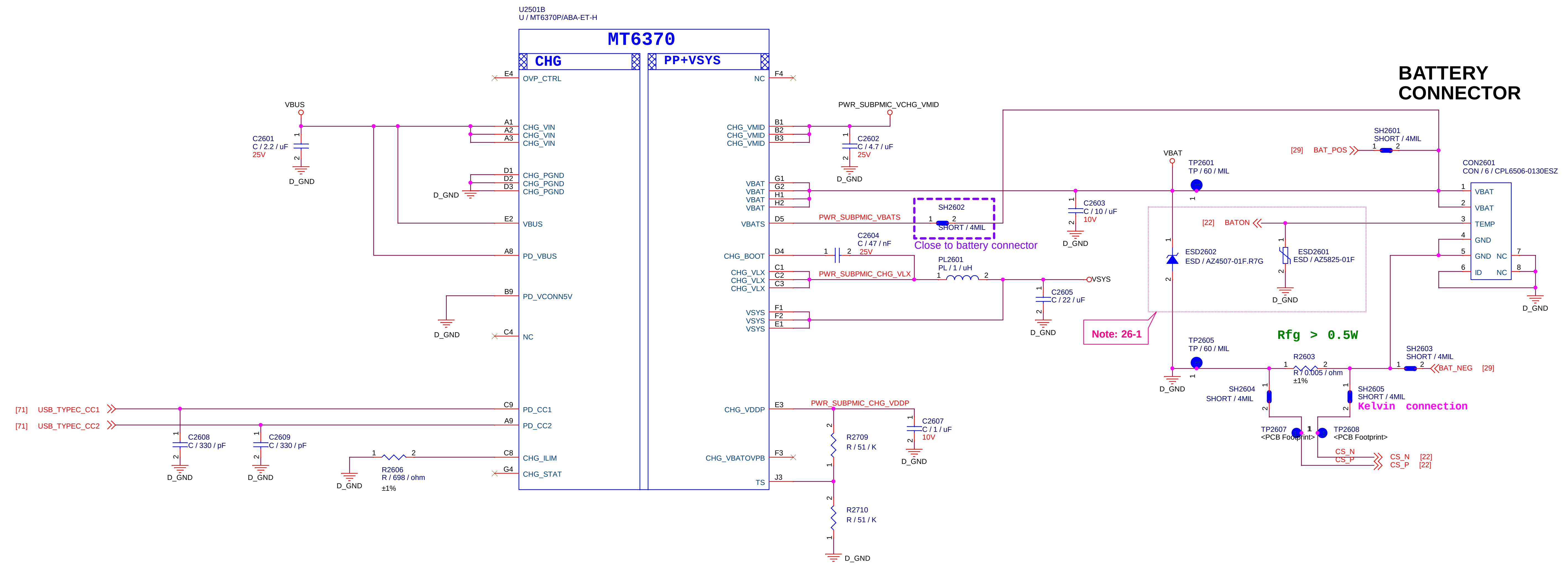


Title
25_POWER_SubPMIC-General

Size C

MTK Confidential

Date: Thursday, January 25, 2018 Sheet 25 of 99



Schematic design notice of "26_POWER_MT6370-Charger + PP" page.

Note 26-1: For better ESD or surge performance we need choose suitable device for system protection. Please refer to [Surge device selection guide V2.0] provide by MTK.

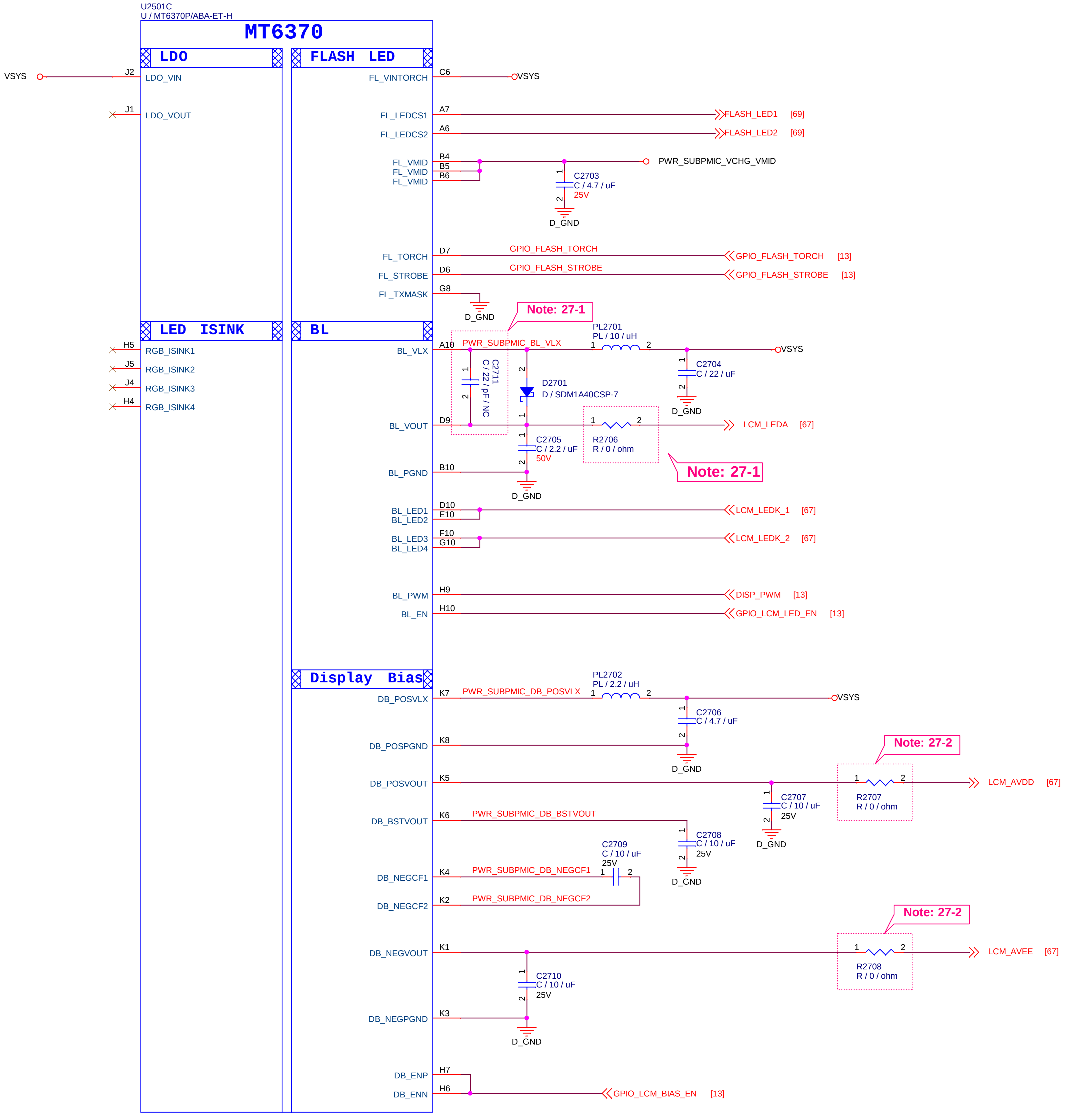
MEDIATEK

Title
26_POWER_SubPMIC-Charger + PP

Size C

MTK Confidential

Date: Thursday, January 25, 2018 Sheet 26 of 99



Schematic design notice of "27_POWER_SubPMIC-HV powers" page.

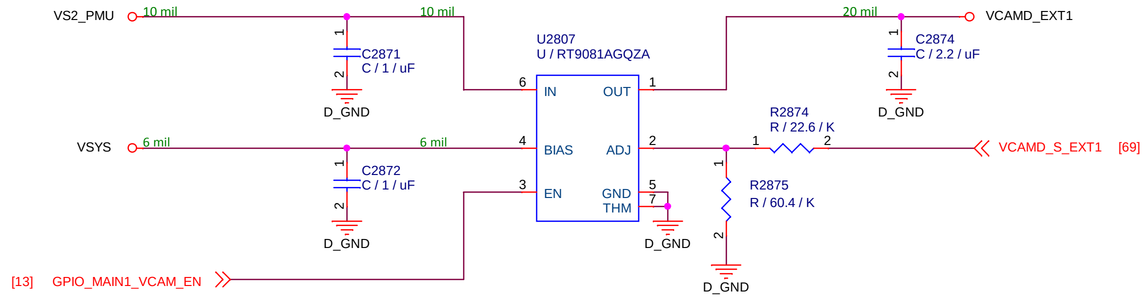
Note 27-1: It is recommended to reserve 0-ohm and cap. for BOM fine tune to minimize RF de-sense.

Note 27-2: It is recommended to reserve 0-ohm for BOM fine tune to minimize RF de-sense.

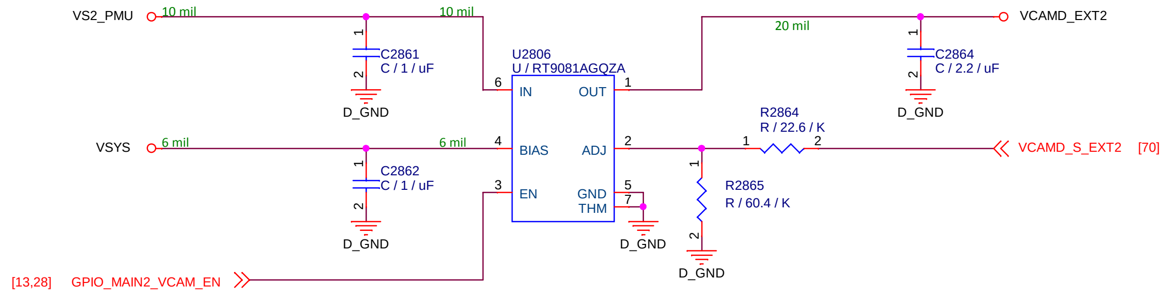
MEDIATEK

Title	27_POWER_SubPMIC-HV powers
Size C	MTK Confidential
Date: Thursday, January 25, 2018	Sheet 27 of 99

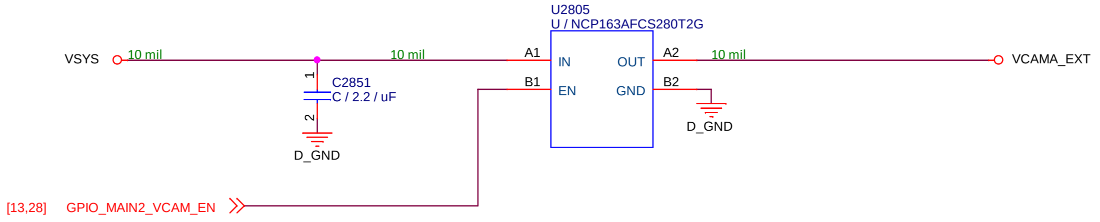
LDO for Rear Camera (VCAMD_EXT1)



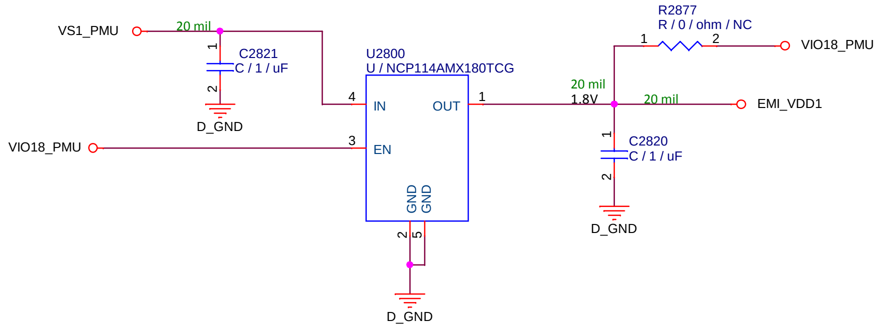
LDO for Rear Camera 2 (VCAMD_EXT2)



LDO for Rear Camera (VCAMA_EXT)



LDO for EMI_VDD1 of LPDDR4X VDD1



MEDIATEK

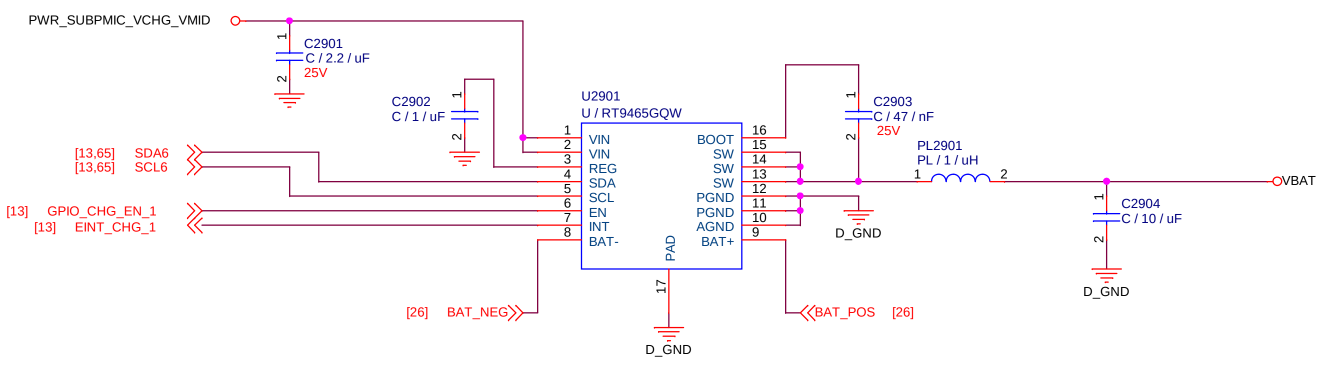
Title
28_POWER_ThirdParty_Powers

Size C

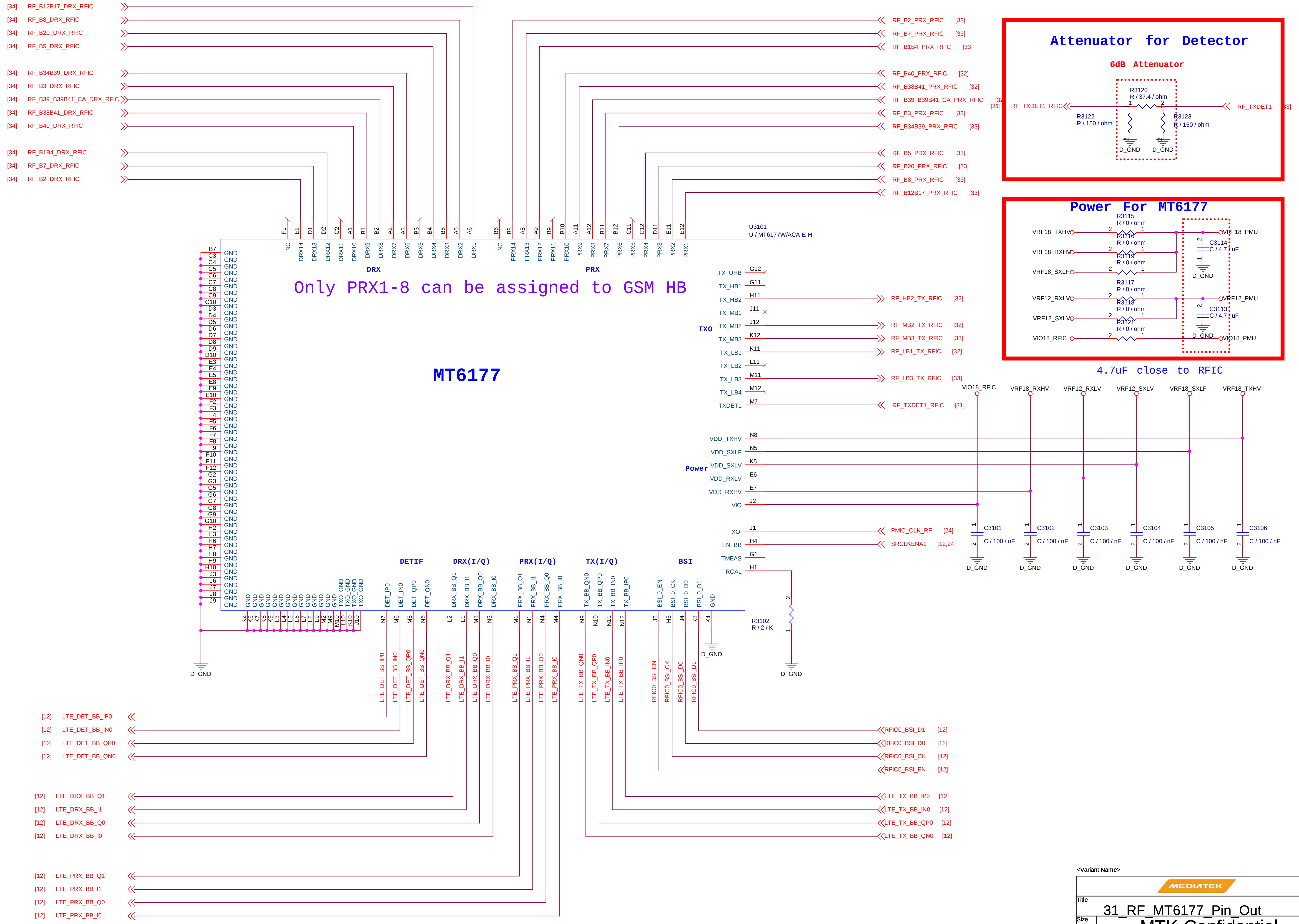
MTK Confidential

Date: Thursday, January 25, 2018 Sheet 28 of 99

Slave Charger RT9465



BAT_POS and BAT_NEG Need Kelvin Connection to Battery Connector



<Variant Name>

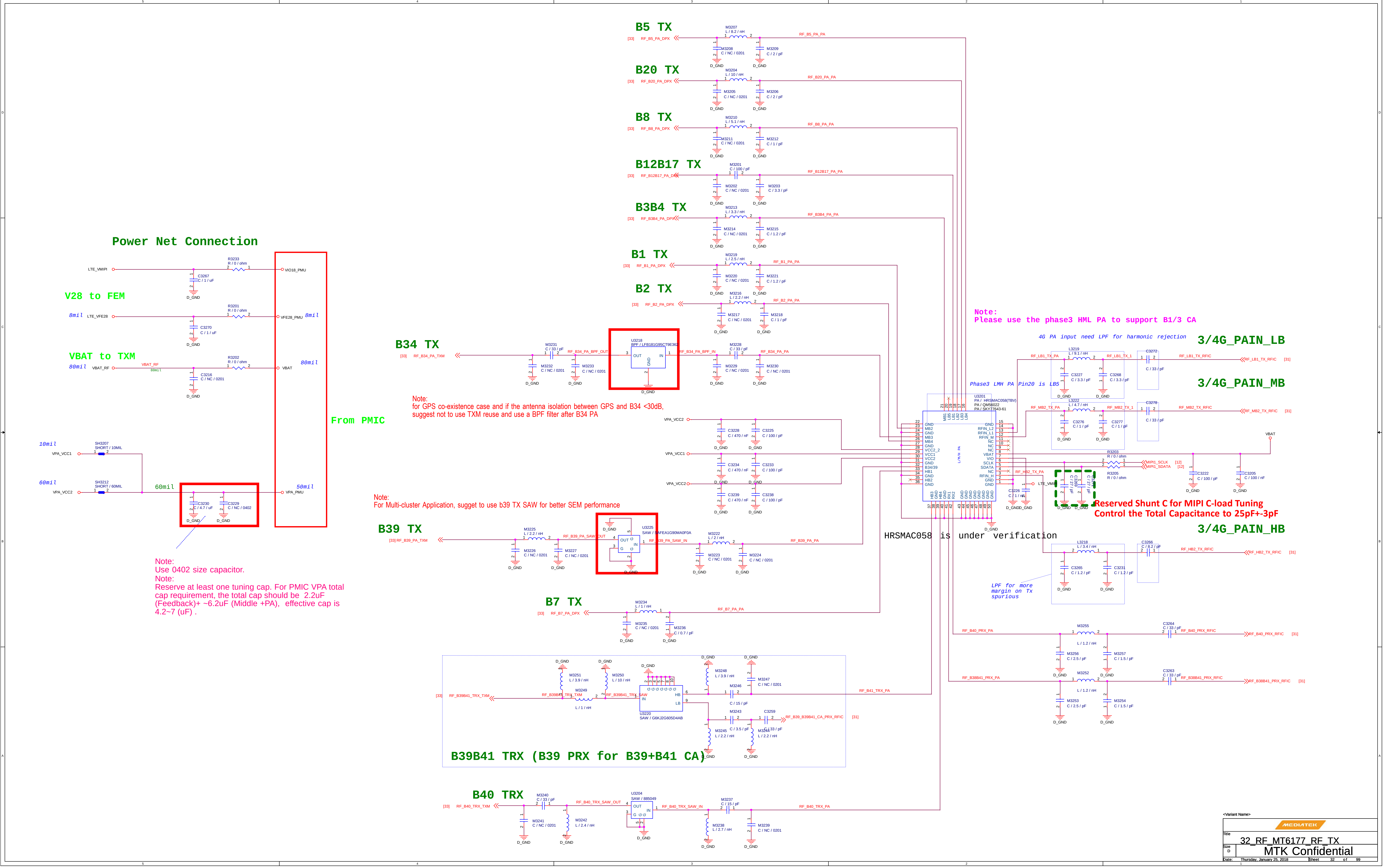
MEDIATEK

Title: 31_RF_MT6177_Pin_Out

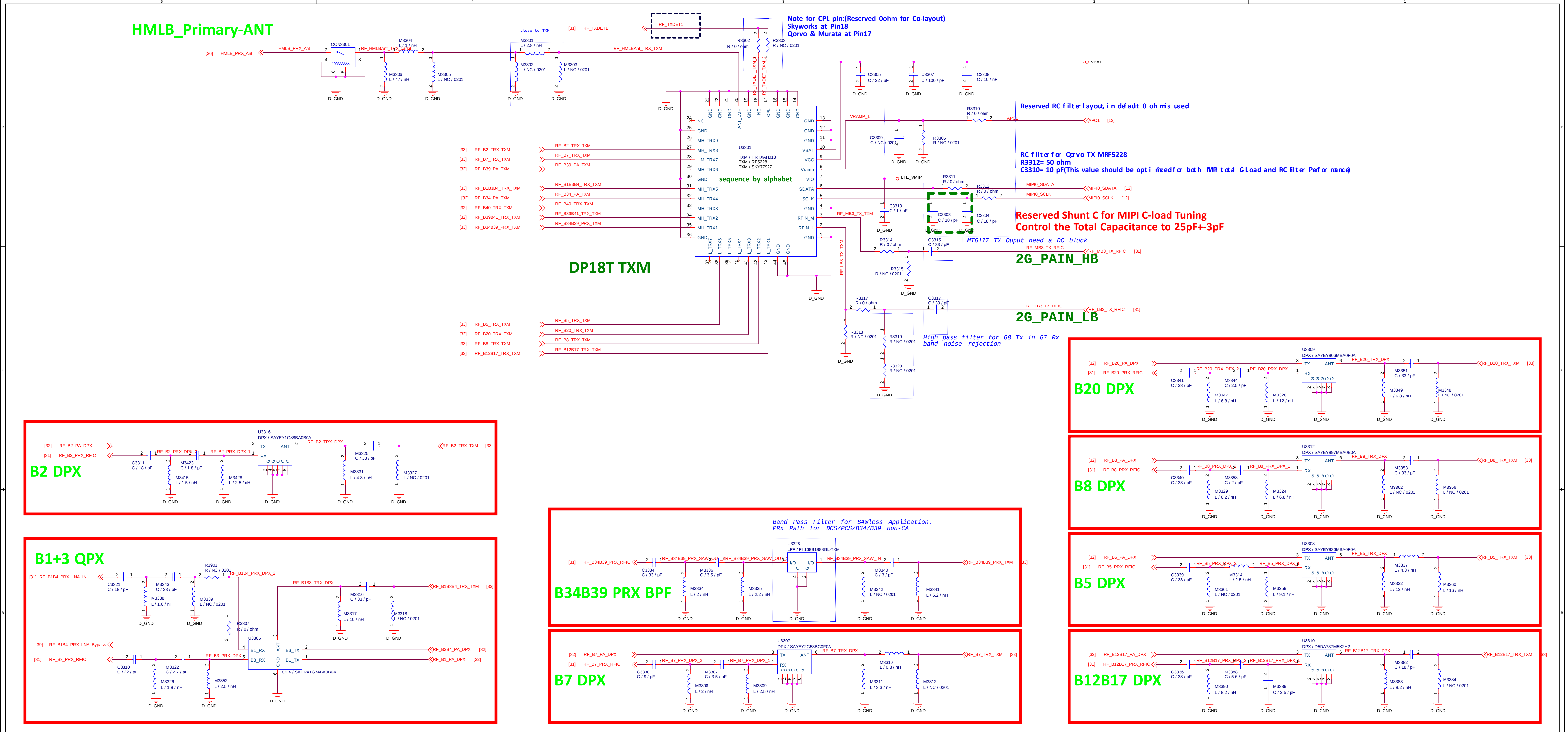
Size: C

MTK Confidential

Date: Thursday, January 25, 2018 Sheet 31 of 99



B5 TX
B20 TX
B8 TX
B12B17 TX
B3B4 TX
B1 TX
B2 TX
B34 TX
B39 TX
B7 TX
B39B41 TRX (B39 PRX for B39+B41 CA)
B40 TRX
Power Net Connection
V28 to FEM
VBAT to TXM
From PMIC
10mil
60mil
8mil
80mil
50mil
Note:
Use 0402 size capacitor.
Note:
Reserve at least one tuning cap. For PMIC VPA total cap requirement, the total cap should be 2.2uF (Feedback)+ ~6.2uF (Middle +PA), effective cap is 4.2~7 (uF) .
Note:
for GPS co-existence case and if the antenna isolation between GPS and B34 <30dB, suggest not to use TXM reuse and use a BPF filter after B34 PA
Note:
For Multi-cluster Application, sugget to use b39 TX SAW for better SEM performance
Note:
Please use the phase3 HML PA to support B1/3 CA
4G PA input need LPF for harmonic rejection
Phase3 LMH PA Pin20 is LB5
3/4G_PAIN_LB
3/4G_PAIN_MB
3/4G_PAIN_HB
U3201
PA / HRSMAC058(TBV)
PA / QM56022
PA / SKY77643-61
HRSMAC058 is under verification
Reserved Shunt C for MIPI C-load Tuning
Control the Total Capacitance to 25pF+-3pF
LPF for more margin on Tx spurious
<Variant Name>
MEDIATEK
Title
32_RF_MT6177_RF_TX
Size D
MTK Confidential
Date: Thursday, January 25, 2018
Sheet 32 of 99



Area	2G	3G	4G	4G Roaming	UL intra-band CA	DL intra-band CA	DL inter-band CA
China	2/3/5/8	1/2/5/8/34/39 /BC0	1/3/5/7/8/34/38/39/40/ 41	4/8/17(12)/20		CCA: 3+3, 38+38, 39+39, 40+40, 41+41 New:1+1(CCA)	1+3, 1+5, 3+5, 39+41,

Supported Band Combination

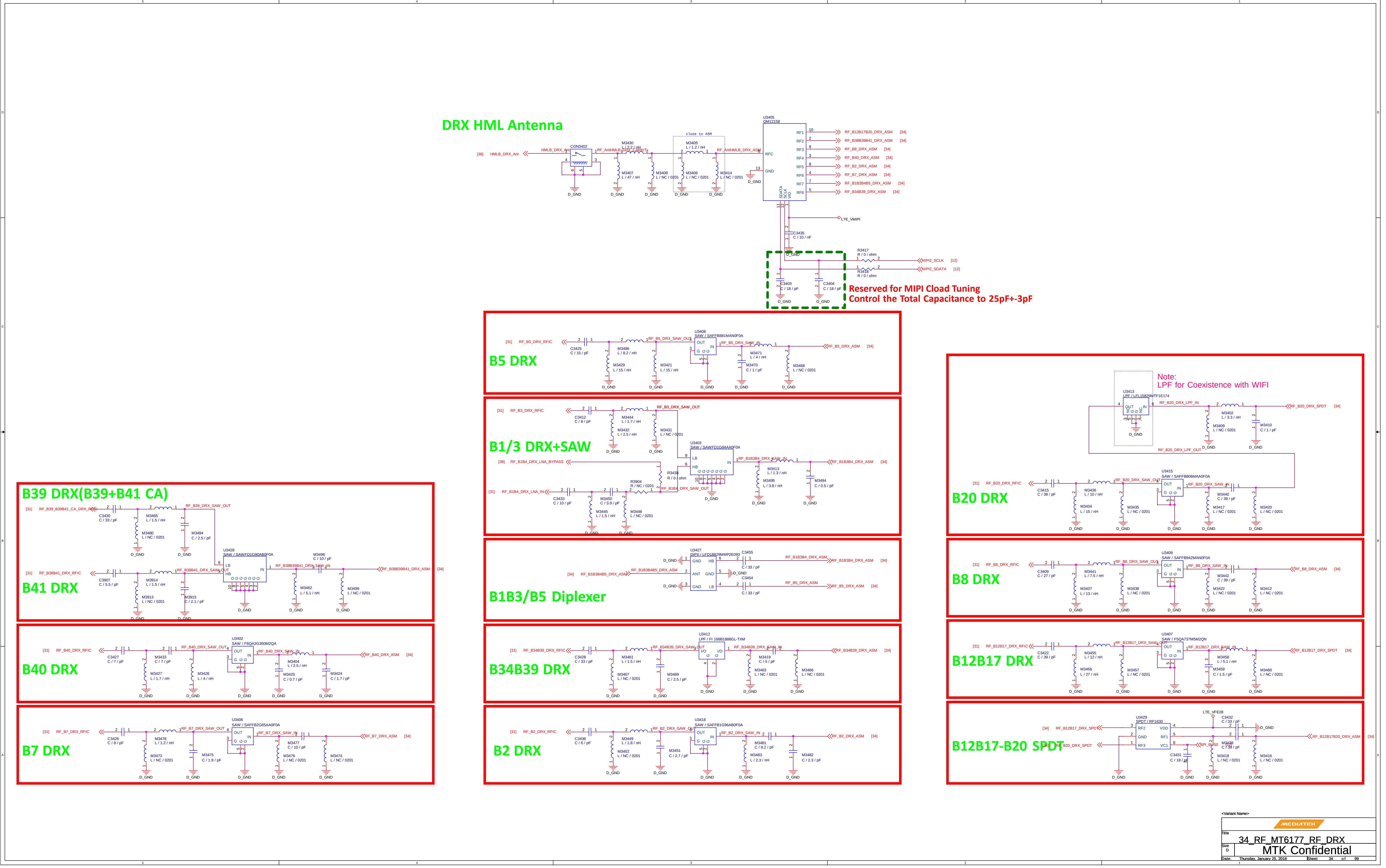
<Variant Name>

MEDIATEK

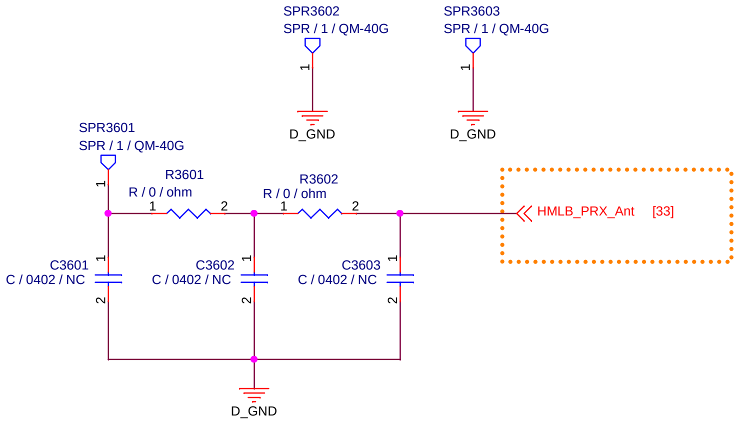
Title: 33_RF_MT6177_RF_PRX

Size: D — MTK Confidential

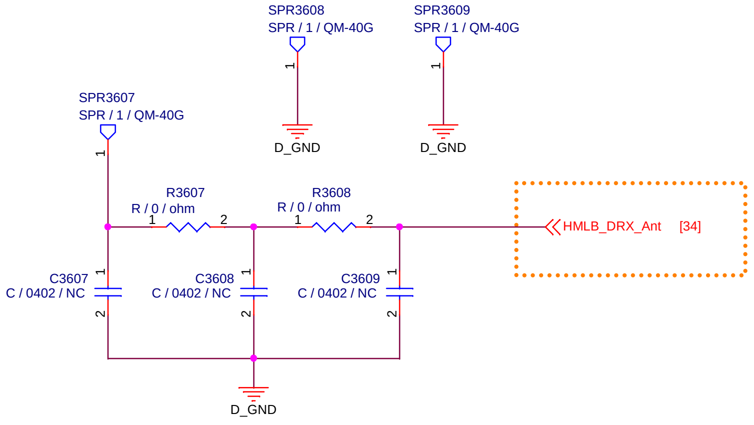
Date: Thursday, January 25, 2018 — Sheet 33 of 99


DRX HML Antenna
close to ASM
U3405
QM12158
LTE_VMIPI
Reserved for MIPI Cload Tuning
Control the Total Capacitance to 25pF+-3pF
B5 DRX
B1/3 DRX+SAW
B39 DRX(B39+B41 CA)
B41 DRX
B40 DRX
B7 DRX
B1B3/B5 Diplexer
B34B39 DRX
B2 DRX
Note:
LPF for Coexistence with WIFI
B20 DRX
B8 DRX
B12B17 DRX
B12B17-B20 SPDT
<Variant Name>
MEDIATEK
Title
34_RF_MT6177_RF_DRX
Size
D
MTK Confidential
Date: Thursday, January 25, 2018
Sheet 34 of 99

MAIN ANT (ANT0)



RXD ANT (ANT1)



MEDIATEK

Title: 36_RF_ANT

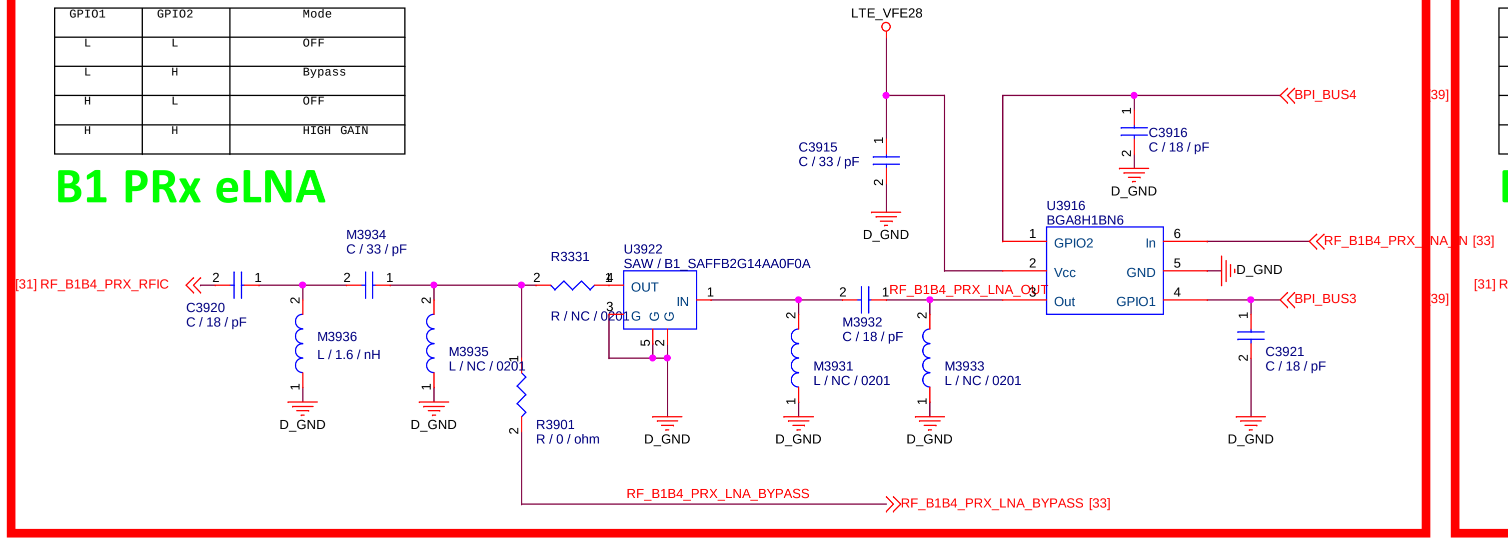
Size: C

MTK Confidential

Date: Thursday, January 25, 2018 | Sheet 36 of 99

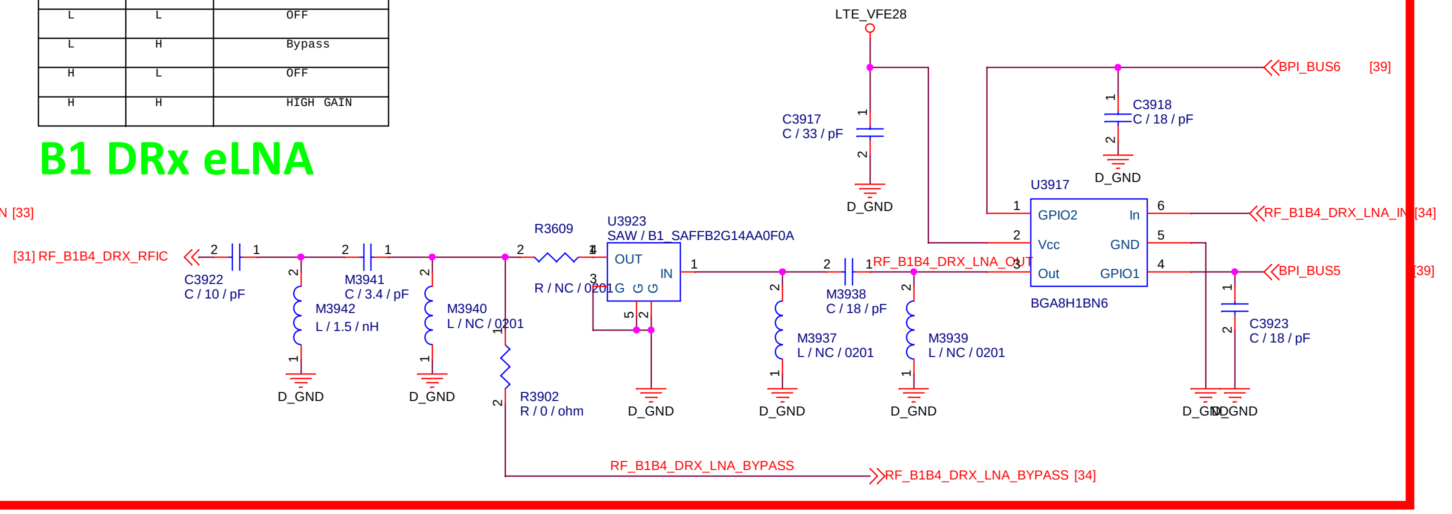
GPIO1	GPIO2	Mode
L	L	OFF
L	H	Bypass
H	L	OFF
H	H	HIGH GAIN

B1 PRx eLNA



GPIO1	GPIO2	Mode
L	L	OFF
L	H	Bypass
H	L	OFF
H	H	HIGH GAIN

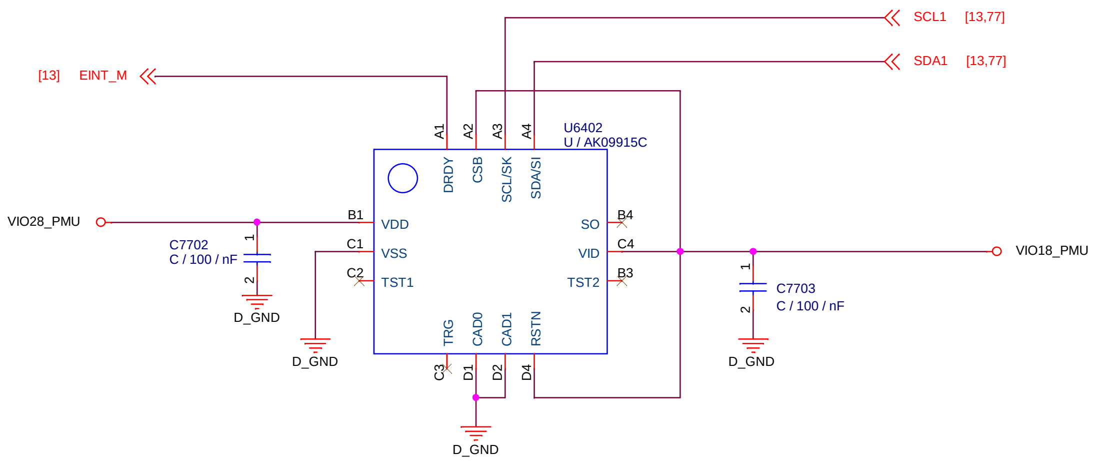
B1 DRx eLNA



Title	<Title>
Size C	Document Number <Doc>	Rev <RevCode>
Date: Thursday, January 25, 2018	Sheet 39 of 99

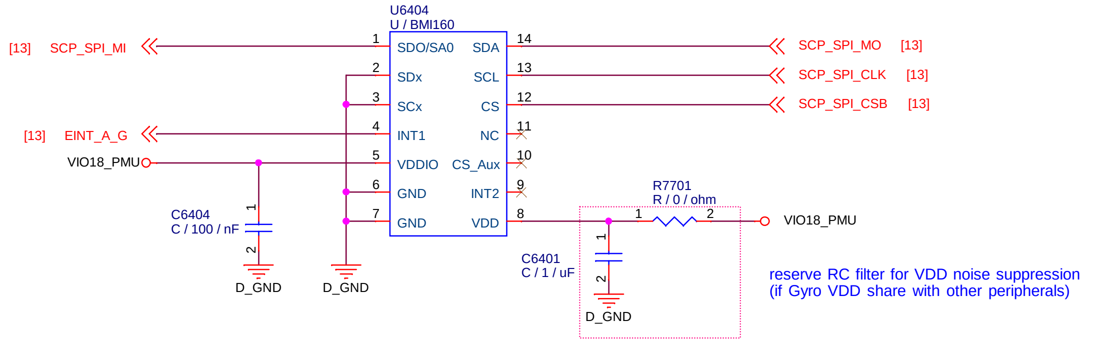
M-Sensor

AK09915 / M-Sensor I2C Address 0x0C (Write: 0x18, Read: 0x19)



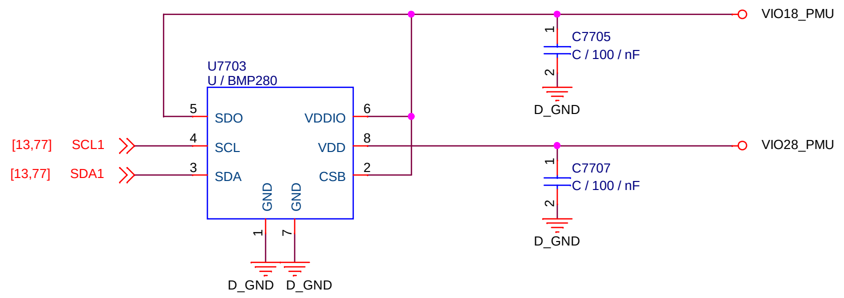
Accerometer + Gyro Sensor

default SPI (if sensor hub support)



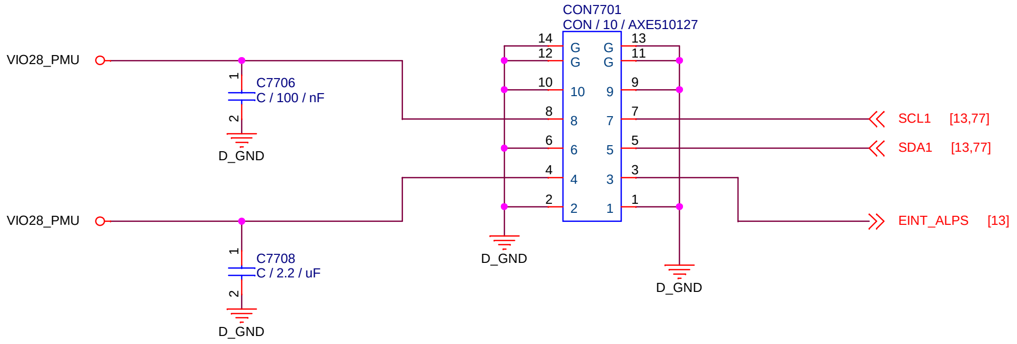
Baro Sensor

Baro I2C address: 0X77 (Write:0xEE, Read:0xEF)



ALS +UV + Proximity Sensor

CM36558 / ALPS + UV I2C address: 0X51 (Write:0xA2, Read:0xA3)



Schematic design notice of "77_PERI_SENSORS_MEMs_ALS/PS" page.

Note 77-1: [M sensor] Keep a minimum distance of 15mm from power ICs / PCB traces of more than 100mA / magnet component. Check HW design notice for more detail

Note 77-2: [A+G] For optmized GPS performance, please check HW design notice for Sensor selection guide

Note 77-3: [A+G] MUST use SPI for optmized sensor hub performance **DO NOT USE i2C**

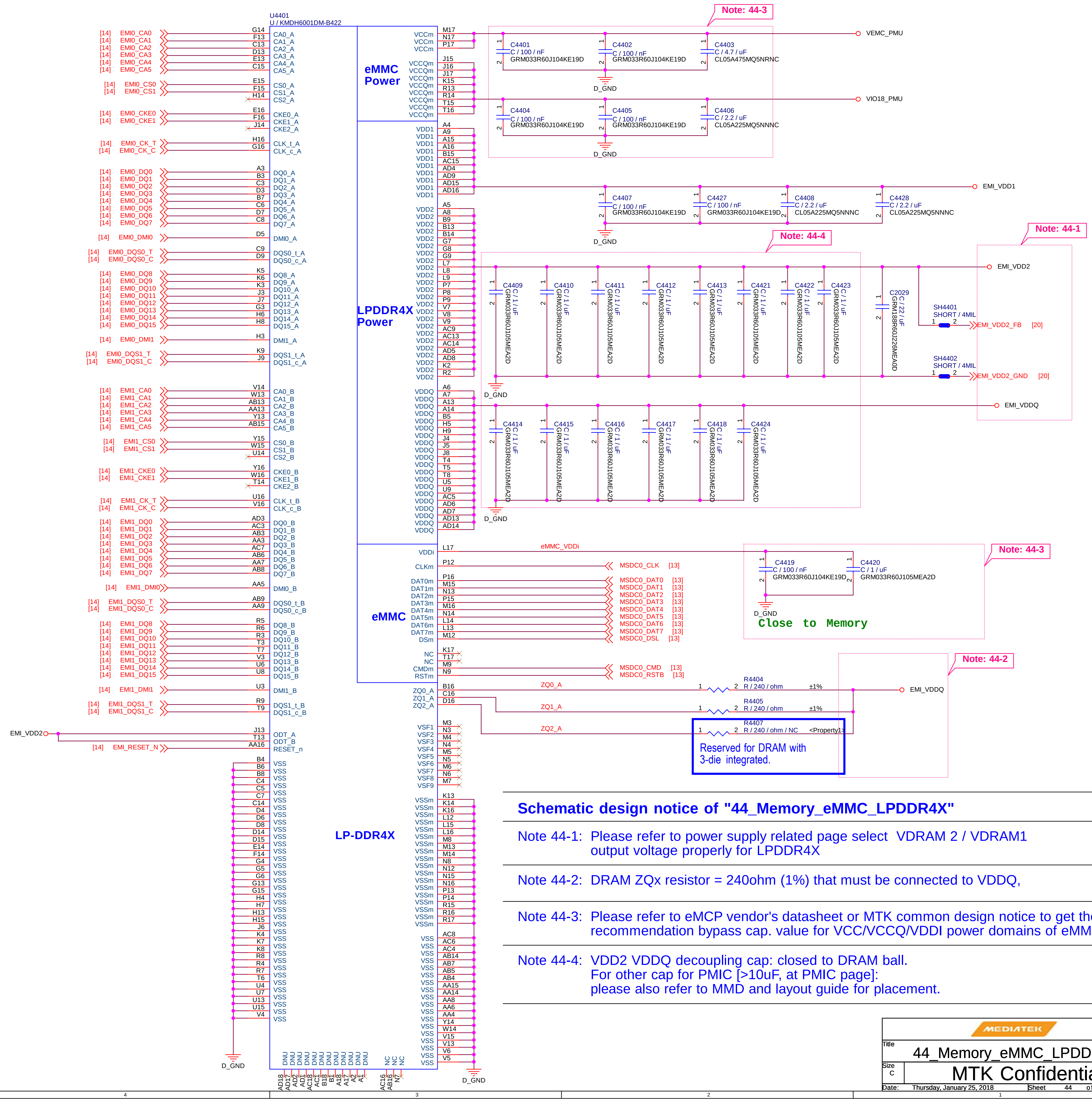
Note 77-4: [A+G] Suggest choose sensor support FIFO watermark interrupt otherwise we cannot support Hifi-sensor, daydream VR. And Sensor-location accuracy will become worse.

Note 77-5: [Baro] Reserve Baro sensor for LPPe feautre (Must for North America Operator / NA SKU)

Note 77-6: DO NOT share Sensor hub i2C to other non-SCP device

Note 77-7: Interrupt pin of MEMS sensor must be assign to ball EINT[12:0]

Title	77_PERI_SENSORS_MEMs_ALS/PS
Size C	MTK Confidential
Date: Thursday, January 25, 2018	Sheet 41 of 42



Schematic design notice of "44_Memory_eMMC_LPDDR4X"

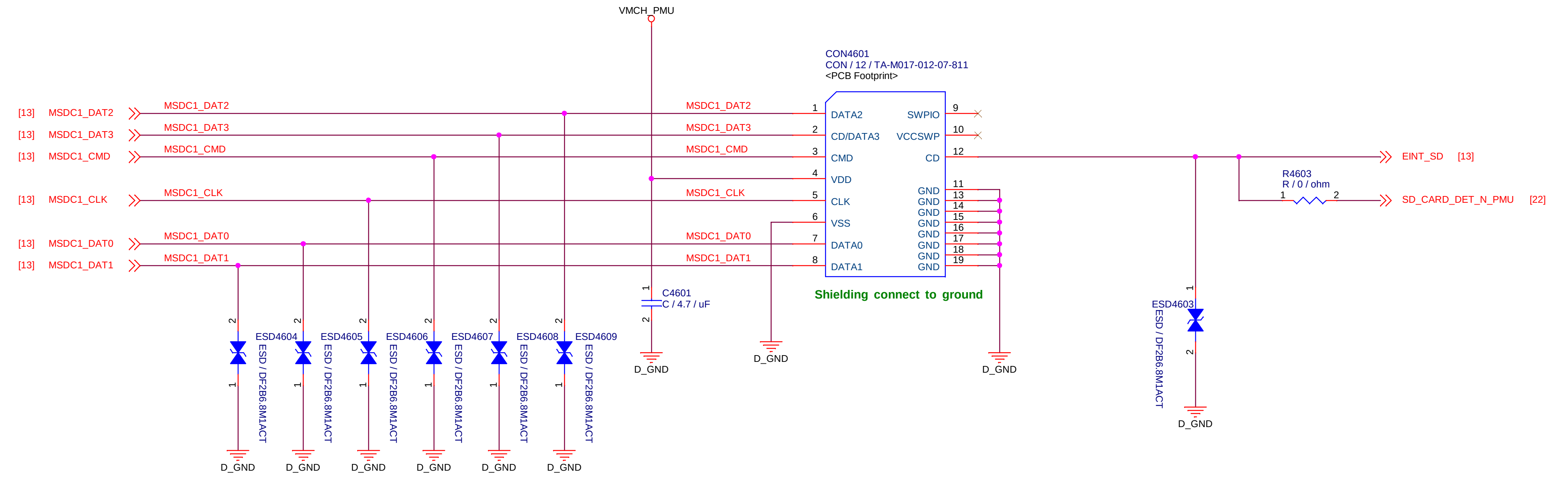
Note 44-1: Please refer to power supply related page select VDRAM 2 / VDRAM1 output voltage properly for LPDDR4X

Note 44-2: DRAM ZQx resistor = 240ohm (1%) that must be connected to VDDQ,

Note 44-3: Please refer to eMCP vendor's datasheet or MTK common design notice to get the recommendation bypass cap. value for VCC/VCCQ/VDDI power domains of eMMC.

Note 44-4: VDD2 VDDQ decoupling cap: closed to DRAM ball.
For other cap for PMIC [>10uF, at PMIC page]:
please also refer to MMD and layout guide for placement.

SD CARD



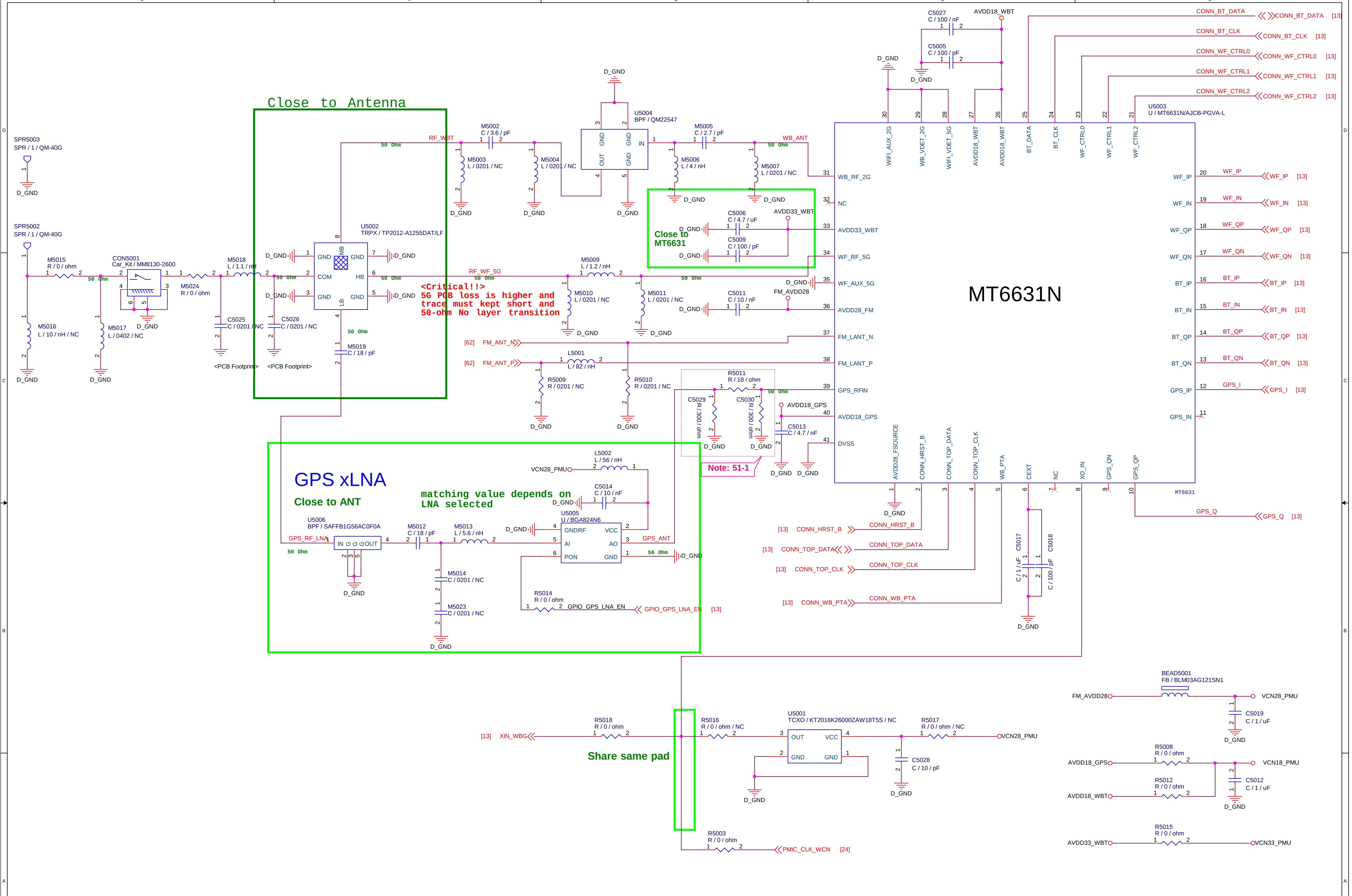
MEDIATEK

Title
46_Memory SD Card

Size
C

MTK Confidential

Date: Thursday, January 25, 2018 Sheet 46 of 99



PMIC R5016/R5017 NC, R5003/R5018 0ohm
TCXO U5001 mounted, R5016/R5017 0ohm mounted, R5003/R5018 NC

Schematic design notice of "51_CONNECTIVITY_MT6631" page.

Note 51-1: Note 51-1: Add 3dB resistor attenuator at external LNA output for more AGC saturation margin. Please let total RF loss < 6dB from external LNA output to GPS chip-input.

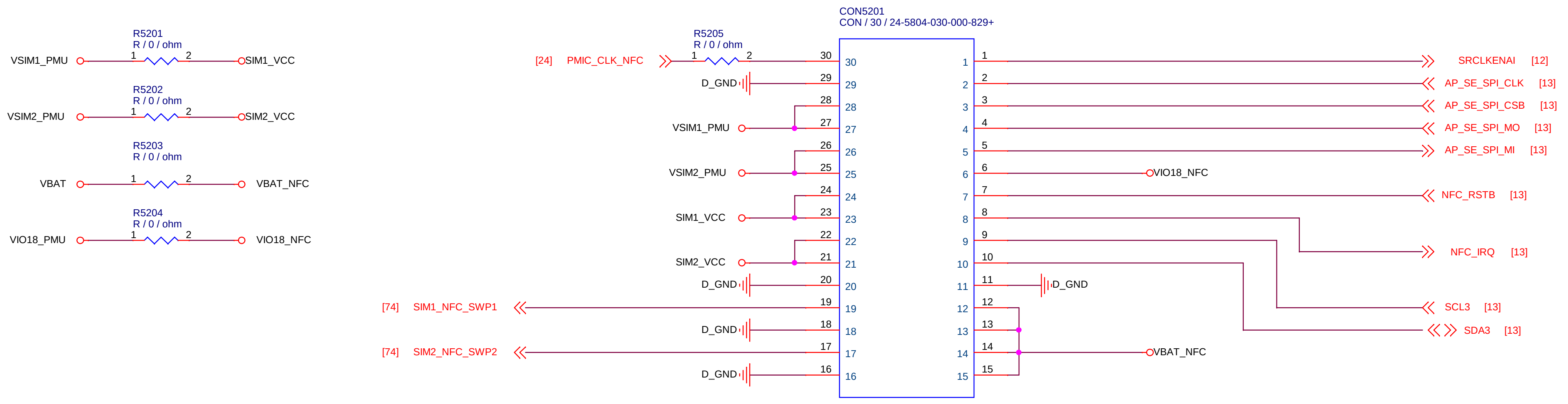
MEDIATEK

Title
51_CONNECTIVITY_CONSYS (A/Ddie)

Size C

MTK Confidential

Date: Thursday, January 25, 2018 Sheet 51 of 99



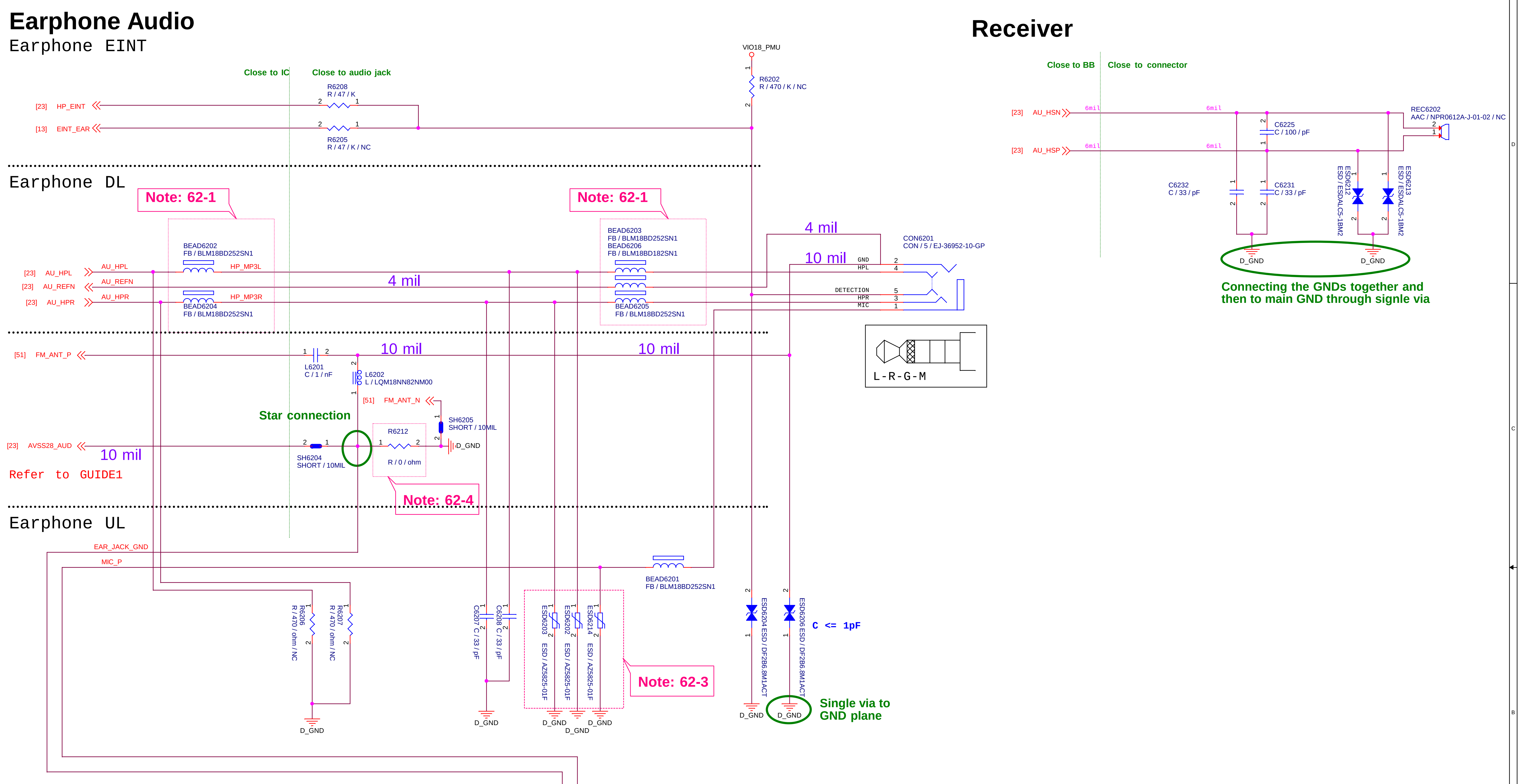
Schematic design notice of "52_CONNECTIVITY_NFC" page.

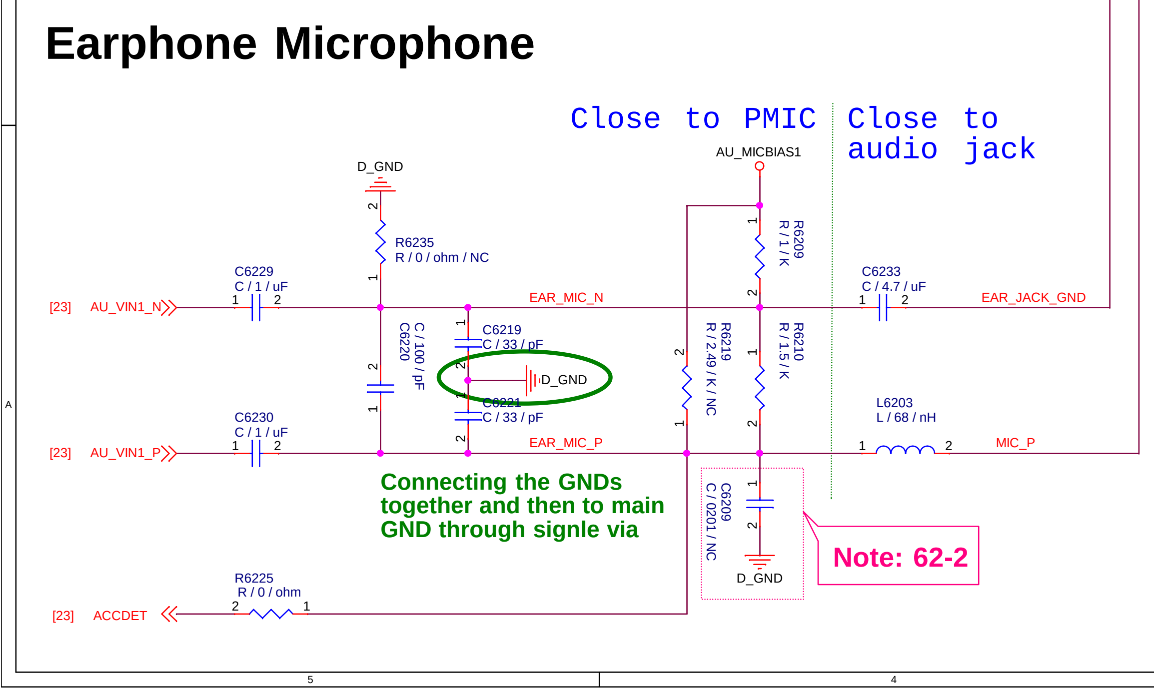
Note 52-1: NFC host I/F and power info are listed in the above connector, NFC COB reference schematic is in the file named "MTK ST NFC Reference Schematic_20170714"

Note 52-2: When NFC is applied, please keep
1. 0ohm NC between VSIM1_PMU and SIM1_VCC
2 0ohm NC between VSIM2_PMU and SIM2_VCC

Note 52-3: When NFC is applied, please follow NFC COB reference schematic to draw NFC COB schematic

Title	52_CONNECTIVITY_NFC
Size C	MTK Confidential
Date: Thursday, January 25, 2018	Sheet 52 of 99





Schematic design notice of "62_PERI_AUDIO_IO" page.

Note 62-1: Part of BEAD6202, BEAD6203, BEAD6204 and BEAD6205 needs changed to "BLM18BD102SN1" for high THD performance (-90dB) but this BOM change will results in FM RSSI 10dB degraded .

Note 62-2: Reserved Cap for CS/RS test, please double check multi-key function when used

Note 62-3: For better ESD or surge performance we need choose suitable device for system protection. Please refer to [Surge device selection guide V2.0] provide by MTK.

Note 62-4:

	Earphone Jack @ Main board	Earphone Jack @ Sub board
R6212	0 ohm	100nF

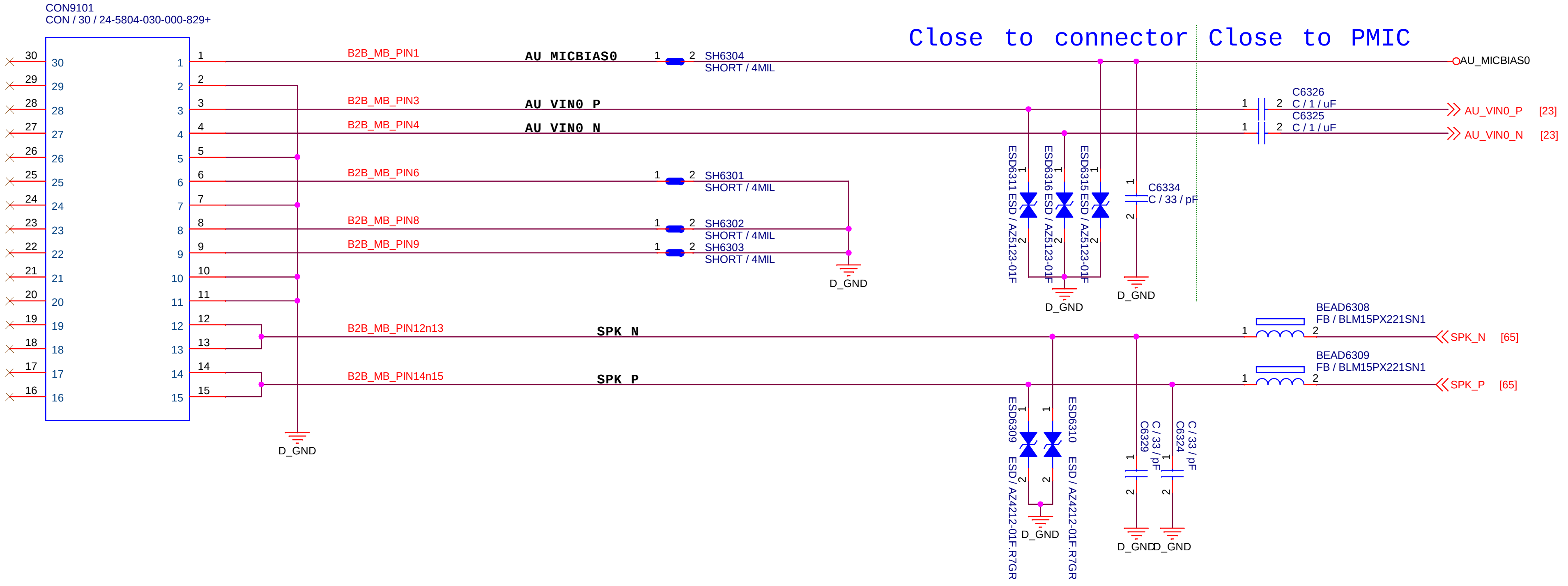
Title: 62_PERI_AUDIO_IO

Size: C

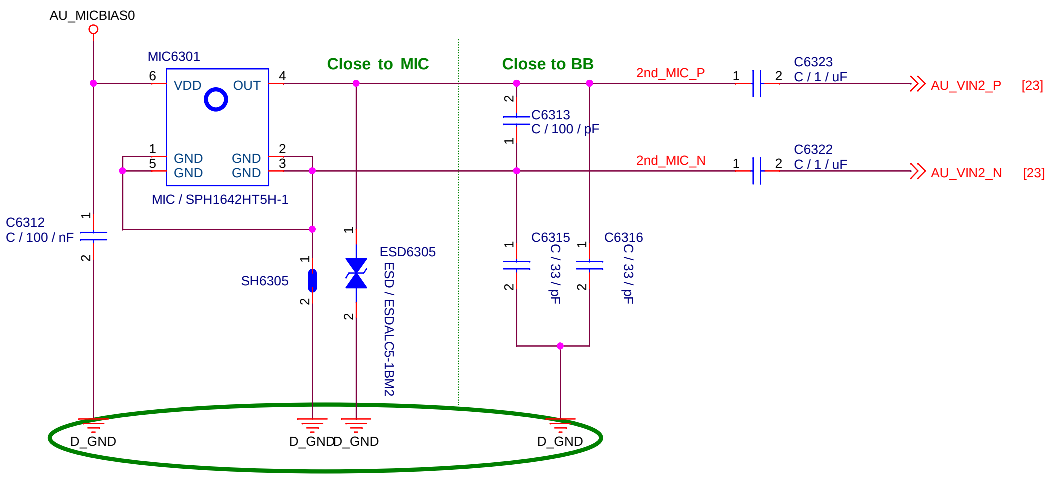
MTK Confidential

Date: Thursday, January 25, 2018 Sheet 62 of 99

Audio/Speech DTB I/F



Handset 2nd Microphone (Rear - DMNR), AMIC



Connecting the GNDs together and then to main GND through signle via

MEDIATEK

Title: 63_PERI_AUDIO_IO2(2 AMIC)

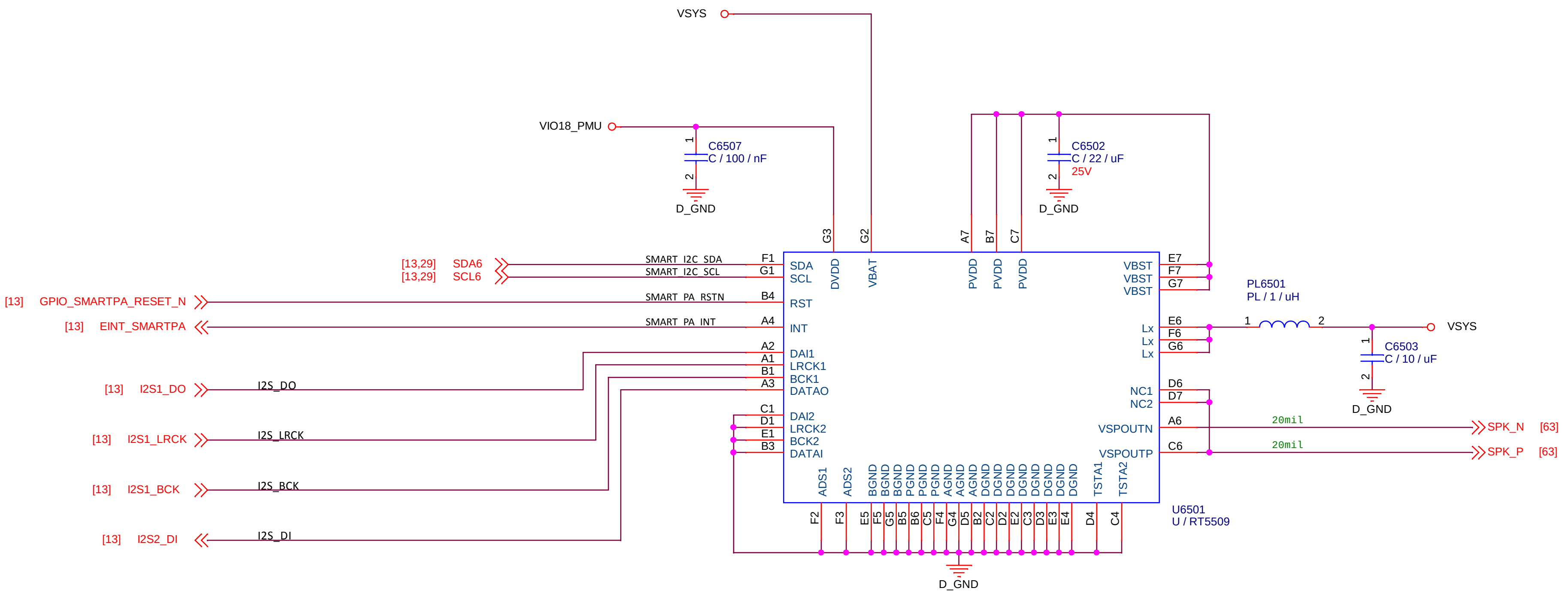
Size: C

MTK Confidential

Date: Thursday, January 25, 2018 Sheet 63 of 99

Speaker Amplifier

RT5509 Speaker AMP I2C Address: 0x34 (Write:0x68, Read:0x69) when ADS1 = GND; ADS2 = GND.



MEDIATEK

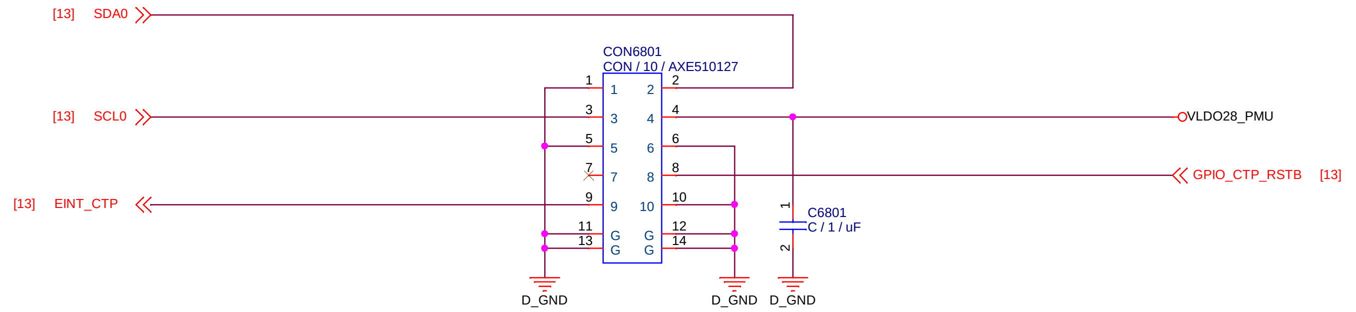
Title
65_PERI_SPEAKER_AMP_RT5509

Size C

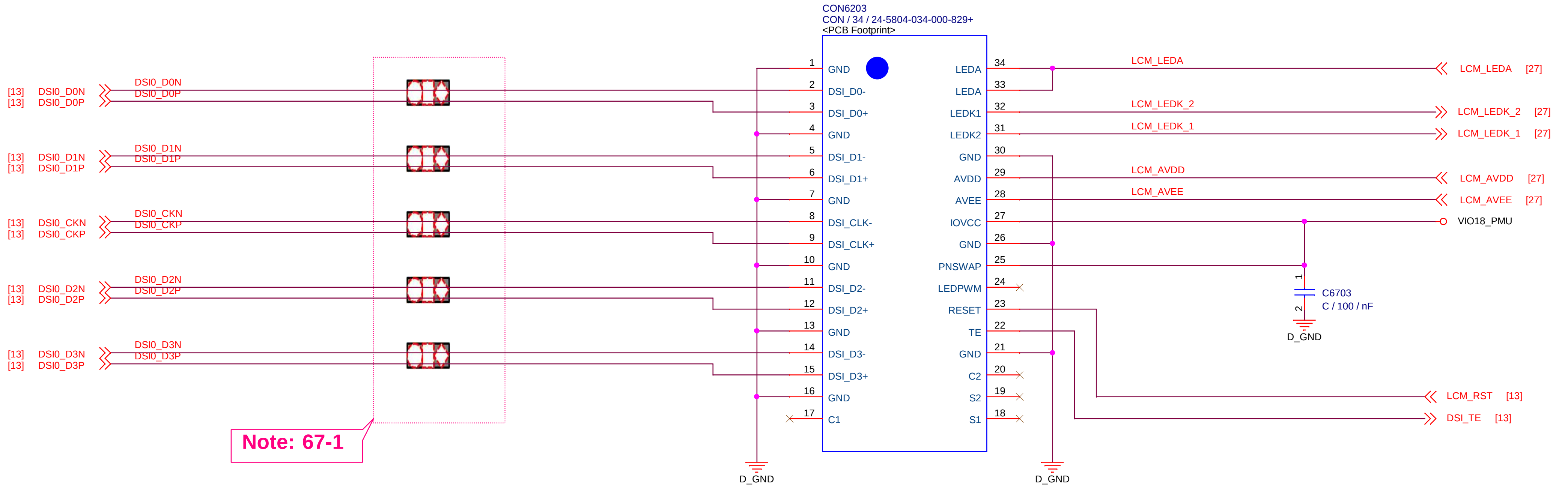
MTK Confidential

Date: Thursday, January 25, 2018 Sheet 65 of 99

CTP



Main LCM



Schematic design notice of "67_PERI_LCD_CTP" page.

Note 67-1: It is recommended to reserve common-mode choke to prevent RF de-sense, the max. cap loading of common-mode choke must be less than 3pF.

MEDIATEK

Title: 67_PERI_LCD_CTP

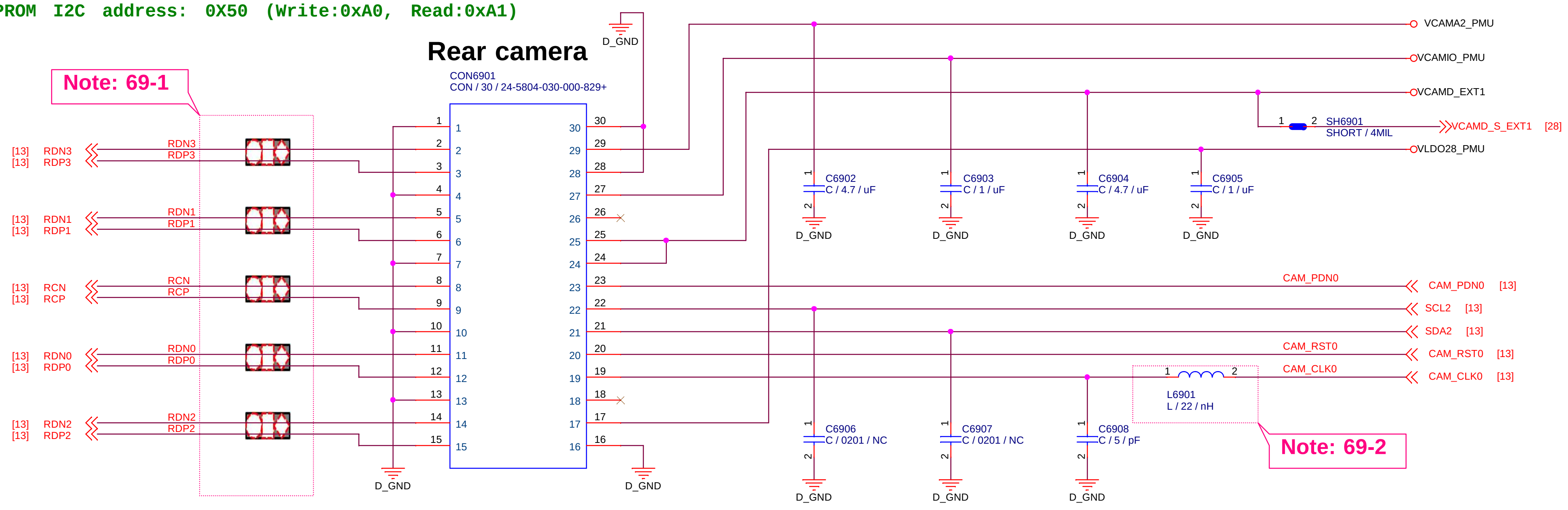
Size: C

MTK Confidential

Date: Thursday, January 25, 2018 Sheet 67 of 99

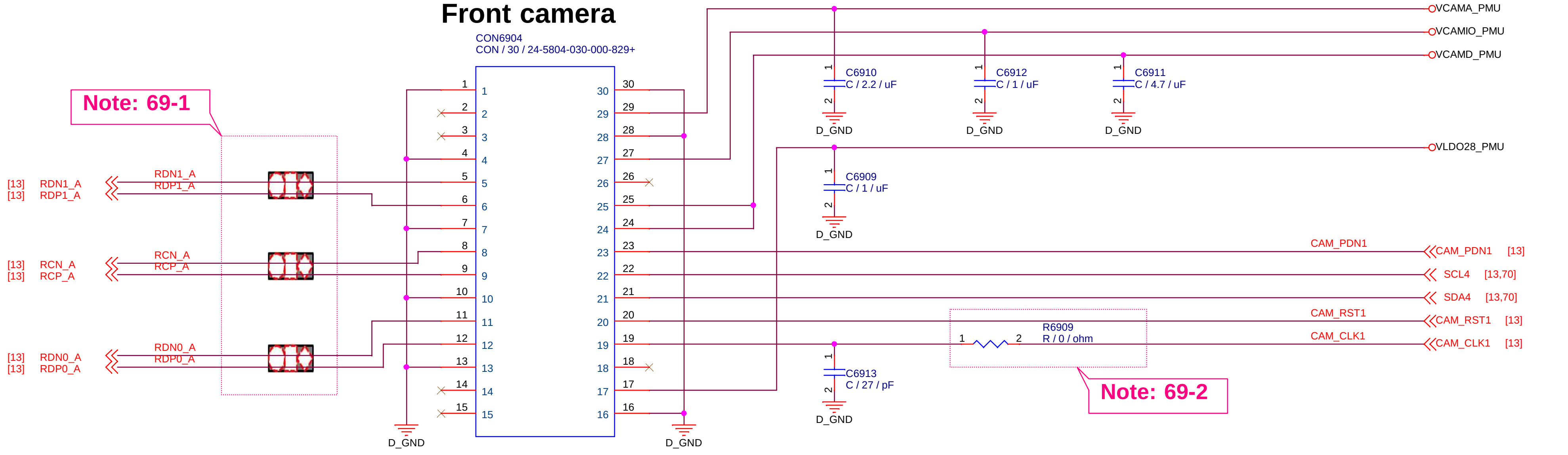
Rear camera I2C address: 0X1A (Write:0x34, Read:0x35)
AF driver I2C address: 0X0C (Write:0x18, Read:0x19)
EEPROM I2C address: 0X50 (Write:0xA0, Read:0xA1)

Rear camera

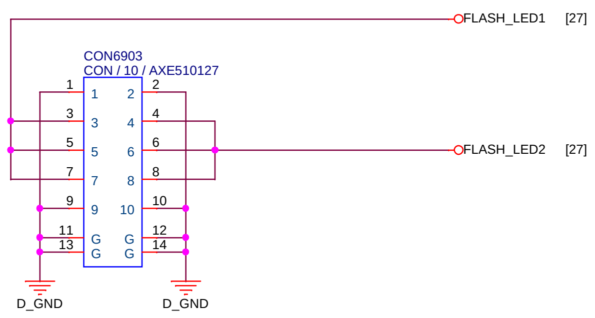


Front camera I2C address:0X35 (Write:0x6A, Read:0x6B)
EEPROM I2C address: 0X54 (Write:0xA8, Read:0xA9)

Front camera



Flash LED



Schematic design notice of "69_PERI_CAMERA" page.

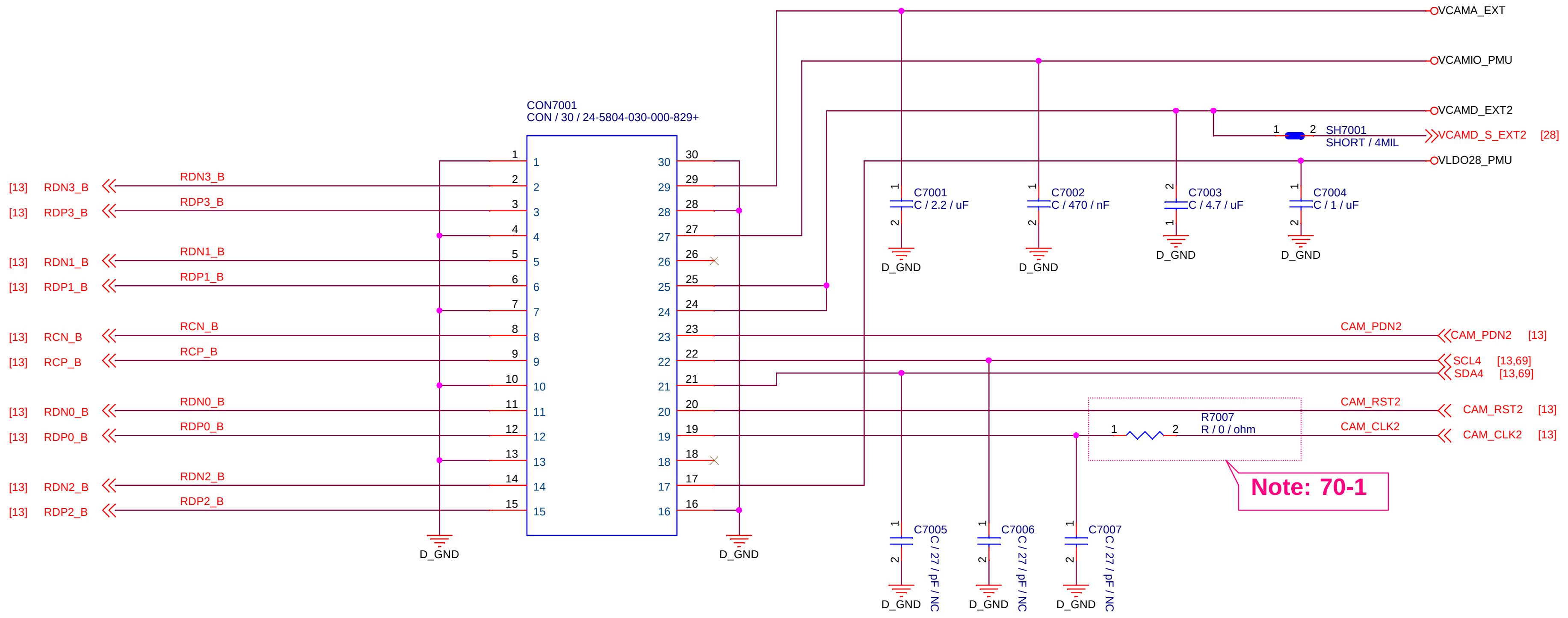
Note 69-1: It is recommended to reserve common-mode choke to prevent RF de-sense, the max. cap loading of common-mode choke must be less than 3pF.

Note 69-2: It is recommended to reserve 0-ohm or inductor for BOM fine tune to minimize RF de-sense.

Title	69_PERI_CAMERA
Size C	MTK Confidential
Date: Thursday, January 25, 2018	Sheet 69 of 1

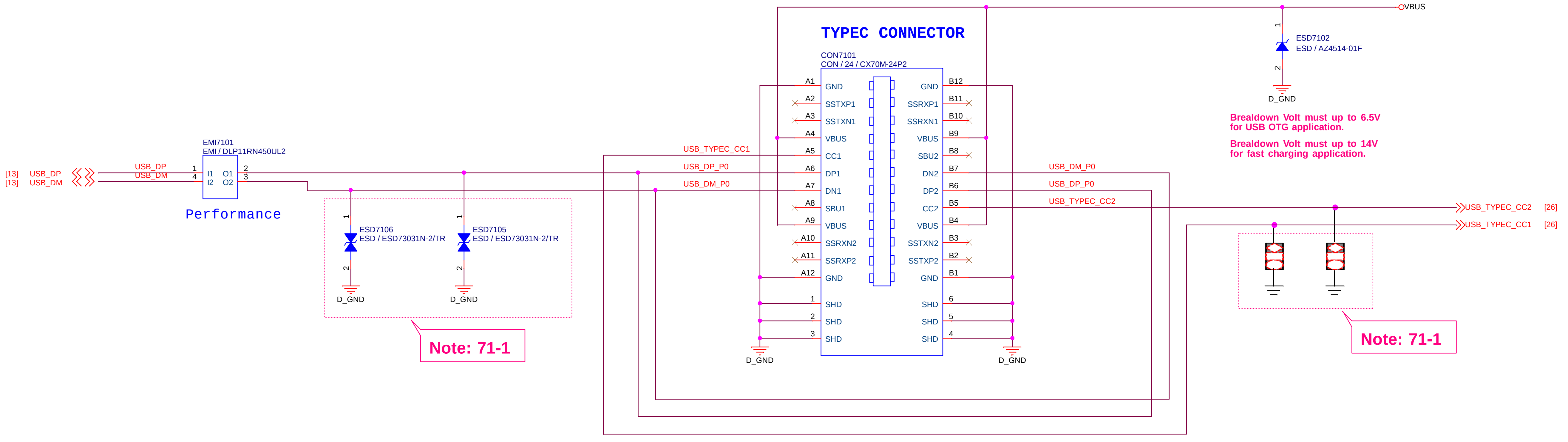
Rear Camera - 2

Rear camera 2 I2C address: TBD (Write:TBD, Read:TBD)
AF driver (TBD) I2C address: TBD (Write:TBD, Read:TBD)



Schematic design notice of "70_PERI_CAMERA_StereoCAM" page.

Note 70-1: It is recommended to reserve 0-ohm for BOM fine tune to minimize RF de-sense.



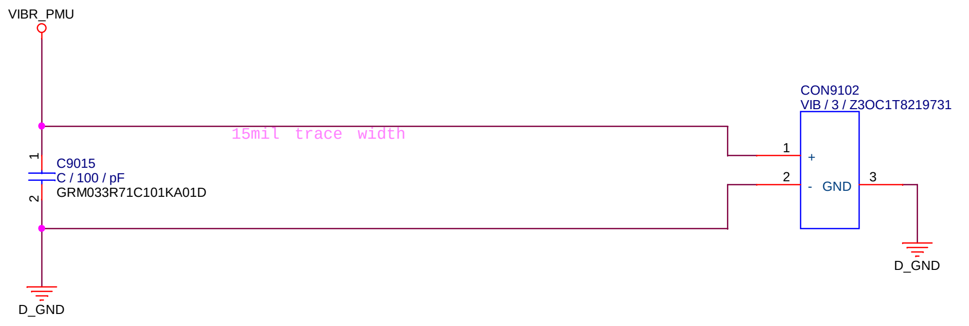
Schematic design notice of "71_PERI_USB 2.0" page.

Note 71-1: For better ESD or surge performance we need choose suitable device for system protection. Please refer to [Surge device selection guide V2.0] provide by MTK.

MEDIATEK

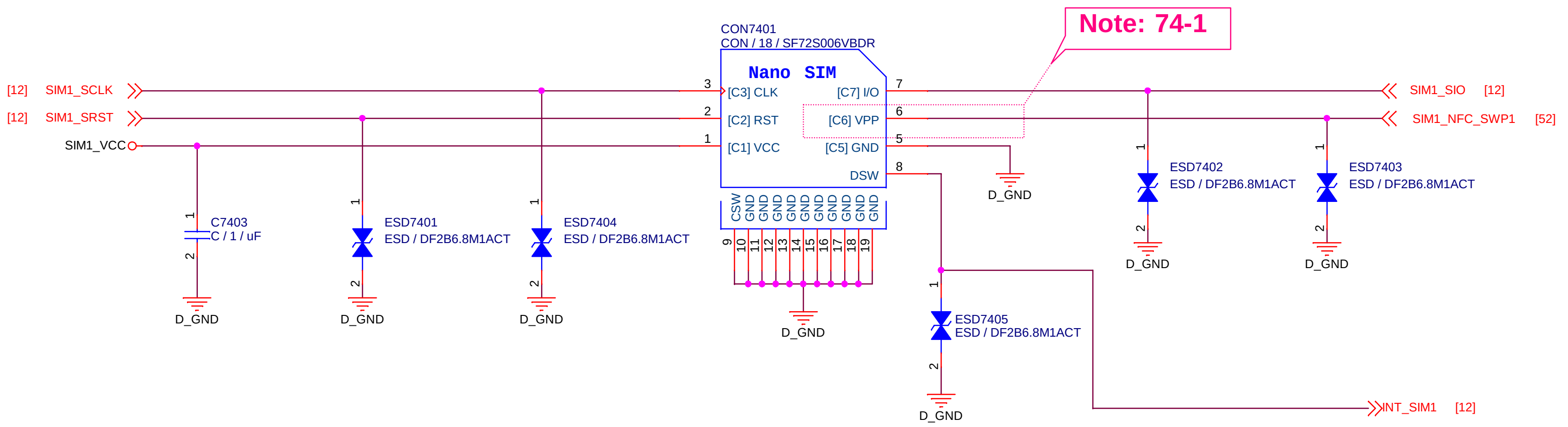
Title	71_PERI_USB 2.0
Size C	MTK Confidential
Date: Thursday, January 25, 2018	Sheet 71 of 99

VIBRATOR

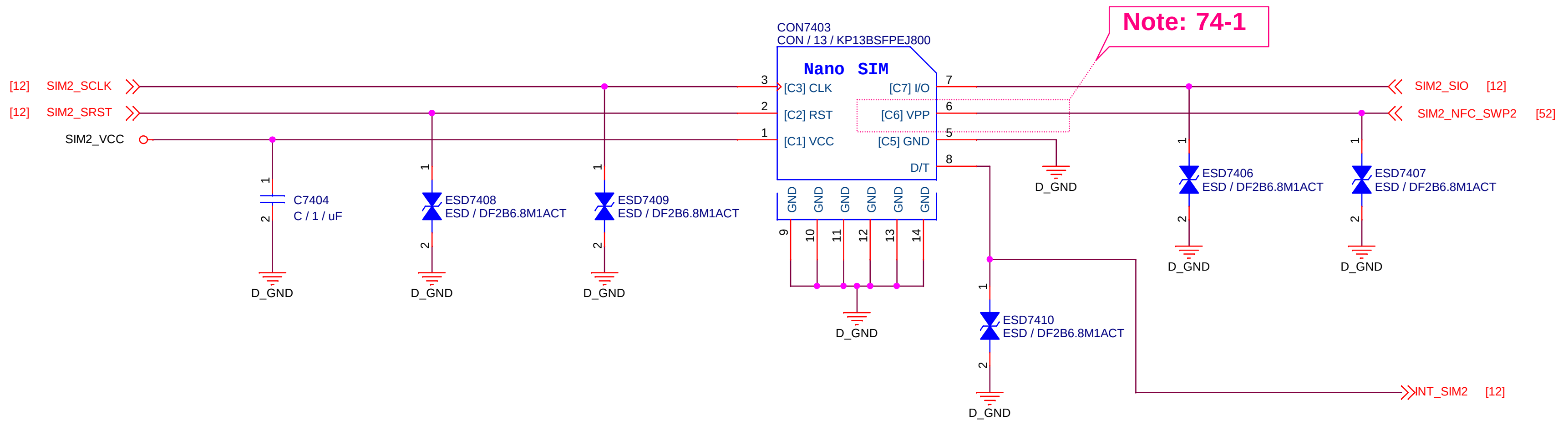


Title
73_PERI_VIBRATOR
Size C
MTK Confidential
Date: Thursday, January 25, 2018 Sheet 73 of 99

SIM1



SIM2



Schematic design notice of "74_PERI_SIM" page.

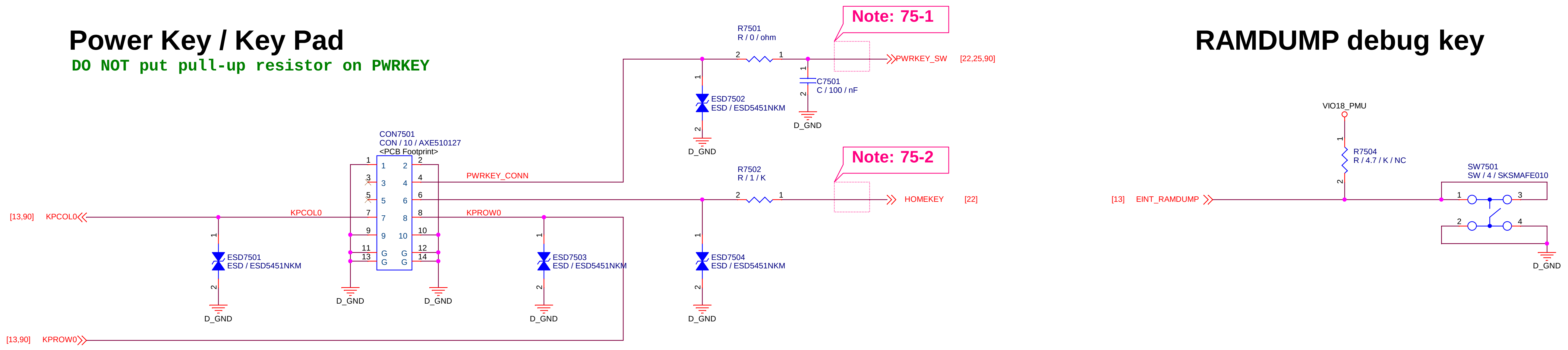
Note 74-1: If do not need NFC SIM function, let Vpp pin floating

Title	74_PERI_SIM
Size C	MTK Confidential
Date: Thursday, January 25, 2018	Sheet 74 of 99

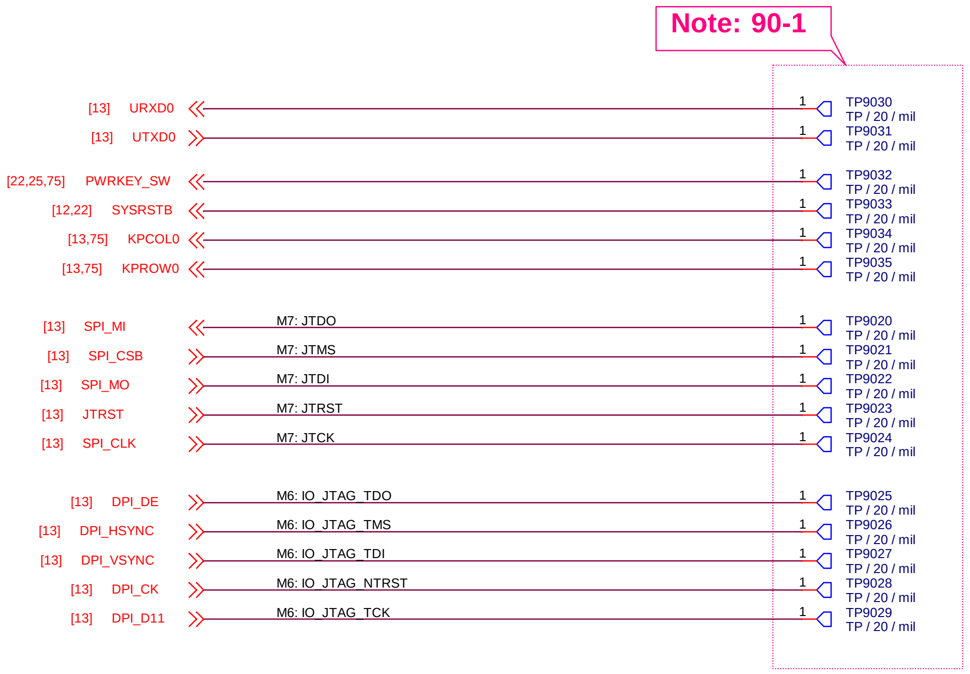
Power Key / Key Pad

DO NOT put pull-up resistor on PWRKEY

RAMDUMP debug key



Schematic design notice of "75_PERI_KEYPAD" page.	
Note 75-1:	DO NOT put pull-up resistor on PWRKEY
Note 75-2:	Volume Up : HOME Key / GND Volume Down : KPROW0/KPCOL0



Schematic design notice of "90_DEBUG_IO" page.

Note 90-1: UART Default support : UART0,
JTAG Default support : AP JTAG, MD_IO_JTAG and C2K_JTAG concurrency with MD_SIB_JTAG

MEDIATEK

Title: 90_DEBUG_IO

Size: C

MTK Confidential

Date: Thursday, January 25, 2018 Sheet 90 of 99